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SCCN: A Time-Effective Hierarchical Interconnection Network for Network-On-Chip

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Abstract

The needed time to send and receive a message among two nodes in an interconnection network has a fundamental role in determining the performance of this network. Therefore, taking a short period of time to send a packet between a source and destination nodes indicates a good performance network with less congestion and latency. Besides, processing data in short-term help in providing fast solutions for many complex problems. Thus, various designs of hierarchical interconnection networks (HINs) for the massively parallel computer (MPC) systems have been presented recently; the main goal of these networks is to replace the conventional ones which showed poor performance in scaling the network size. A Shifted Completely Connected Network (SCCN) proposed as a new HIN topology. Several basic modules (BMs) interconnected hierarchically to create advanced levels networks based on this topology. The structural design and a proposed routing protocol of SCCN discussed in this paper. However, the foremost focus of this work is to evaluate the time cost-effectiveness factor (TCEF) of SCCN in different levels in order to examine the effect of expanding the size of the network on the TCEF. Therefore, the TCEF for the higher levels of SCCN from level (1) to level (3) will be assessed to examine whether SCCN is an effective network in term of time. In addition, the obtained results from each level will be compared to other networks to prove the preeminence of the proposed topology.

Keywords

Author Keywords: Shifted Completely Connected Network (SCCN); Network-on-Chip (NOC); Interconnection Networks; Hierarchical Interconnection Networks (HINs); Static Network Performance; Time Cost-Effectiveness Factor (TCEF); Cost-Effective Factor (CEF); Massively Parallel Computer (MPC) Systems

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