Design and analysis of a boosted pierce oscillator using MEMS SAW resonators

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Abstract

This paper highlights the design and analysis of a pierce oscillator circuit for CMOS MEMS surface acoustic wave resonators. The boosted pierce topology using two, three-stage cascode amplifiers provides sufficient gain to counteract the high insertion losses of − 65 dB at 1.3 GHz of the SAW resonator. For accurate prediction of the oscillator's performance before fabrication, circuit design utilized touchstone S2P measurement results of the MEMS SAW resonator, which provides better results compared to the conventional method of using equivalent circuit simulations. This circuit was designed using Silterra's 0.13 µm CMOS process. It has low power consumption of 1.52 mW with high voltage swing 0.10–0.99 V. All simulations were conducted using Cadence Design Systems and results indicate that phase noise of 92.63 dBc at 1 MHz.

Notes

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