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TECHNICAL PAPER



Design and analysis of a boosted pierce oscillator using MEMS SAW resonators

Mohd Haidar Hamzah¹ · Jamilah Karim² · Aliza Aini Md Ralib³ · Anis Nurashikin Nordin³

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Abstract

This paper highlights the design and analysis of a pierce oscillator circuit for CMOS MEMS surface acoustic wave resonators. The boosted pierce topology using two, three-stage cascode amplifiers provides sufficient gain to counteract the high insertion losses of -65 dB at 1.3 GHz of the SAW resonator. For accurate prediction of the oscillator's performance before fabrication, circuit design utilized touchstone S2P measurement results of the MEMS SAW resonator, which provides better results compared to the conventional method of using equivalent circuit simulations. This circuit was designed using Silterra's 0.13 μ m CMOS process. It has low power consumption of 1.52 mW with high voltage swing 0.10–0.99 V. All simulations were conducted using Cadence Design Systems and results indicate that phase noise of 92.63 dBc at 1 MHz.

1 Introduction

The usage of acoustic wave oscillators has been dominant in the past decades for all communication and networking systems. Cutting-edge research in this field utilize oscillator topologies enhanced with integrated micromechanical resonator devices (Yuan et al. 2015; Li et al. 2016). The usage of MEMS-based resonators is a popular alternative to replace off-chip, conventional quartz resonators. Advancement in integrated circuit fabrication techniques allows MEMS resonators to be miniaturized in order to better address the form-factor needs of RF wireless

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³ Department of Electrical and Computer Engineering, Kulliyyah of Engineering, International Islamic University, Kuala Lumpur, Malaysia devices. A dominant plus factor of silicon MEMS resonators is the fact that it can be integrated together with its feedback CMOS circuitry on a single chip, reducing circuit board area considerably. MEMS based resonators provide high Q factors of more than 1000 in GHz operating frequency range (Yuan et al. 2015; Li et al. 2016; Lavasani et al. 2015; Li et al. 2013, 2015). Monolithic integration and small form factors, make MEMS resonators extremely desirable for multiband wireless systems where they can function as frequency references and RF signal processing filters and mixers (Karim and Nordin 2016).

Typically, MEMS resonators rely on either piezoelectric or capacitive actuation to produce resonant vibrations. Piezoelectric resonators utilize electromechanical coupling capabilities of piezoelectric materials to transform electrical signals into mechanical acoustic waves that vibrate at the frequency of interest. Compared to capacitive actuation, piezoelectric resonators have lower motional resistance, higher power handling capabilities and are capable of generating acoustic waves suitable for radio frequency (RF) applications (Karim and Nordin 2016). MEMS acoustic wave resonators can be categorized into either bulk acoustic wave (BAW) (Gong et al. 2012; Gill and Prasad 2016; Ruffieux et al. 2014) or surface acoustic wave (SAW) resonators (Nordin and Zaghloul 2007; Ralib and Nordin 2014; Ralib et al. 2014; Neculoiu et al. 2009) depending on the direction of the propagating waves. Of late, there have been efforts to make these acoustic wave devices compatible to silicon to achieve a single chip solution (Gong et al. 2012; Rinaldi et al. 2010; Gill and Prasad 2016; Ruffieux et al. 2014; Sankaragomathi et al. 2013; Roy et al. 2016; Nordin and Zaghloul 2007; Ralib and Nordin 2014; Ralib et al. 2014; Neculoiu et al. 2009). However, the performance in terms of frequency-quality factor still need to be improved before it can be marketed for RF applications. The choice of piezoelectric thin film material is crucial to the performance of silicon compatible MEMS acoustic resonators (Morkoç 2008; Hashimoto et al. 2009; Campanella 2010; Bassiri-Gharb 2008).

In recent years, most MEMS based oscillators designed were in MHz range (Li et al. 2016; Lavasani et al. 2015; Li et al. 2013, 2015; Karim and Nordin 2016). Higher losses of MEMS resonators are major restrictions in designing MEMS based oscillators. Thus proper design of amplifier is necessary in order to obtain low noise, low power and high gain. Previous work on MEMS based SAW oscillator has been published in Karim and Nordin (2016), however this oscillator generates higher noise and has limited oscillation amplitude. Recent research has shown several of MEMS based oscillators topologies (Enz et al. 2013; Chengjie et al. 2011; Uranga et al. 2015; Seth et al. 2012; Salvia et al. 2010), but none of them were based on MEMS surface acoustic wave (SAW) resonators.

An example of an oscillator circuit for MEMS resonator is a differential oscillator circuit topology where two symmetrical oscillator cores were cross-coupled to a bulk acoustic wave resonator to produce quadrature signal. High output resistance can be achieved through the cross coupled transistor pair. This topology results in higher amplitude swings and better supply rejection (Rai and Otis 2008). Single transistor pierce oscillator circuit topology is also well-known and had been successfully connected to AIN contour mode MEMS resonator to produce oscillation between 175.4 and 481.56 MHz (Zuo et al. 2010).

In this proposed work, the challenge lies in designing a sustaining amplifier for a high loss CMOS MEMS SAW resonator with Q factors of less than 800 and insertion loss of 65 dB. To deal with this, a promising approach is suggested. The oscillating circuit comprises of cascode connections of two three-stage amplifiers. Stacking amplifiers will enable high transconductance, *gm* from both stages thus leading to an increment on the gain boost. The configuration is constructed as such in order to recoup with the insertion loss of SAW without compromising voltage overdrive consideration limitation.

This paper is divided into four main parts; Sect. 2 is the MEMS SAW resonator equivalent circuit model; Sect. 3 describes the boosted pierce circuit design architecture; Sect. 4 elaborates the outcomes of SAW S21 insertion loss and transient analysis of the boosted pierce circuit and

finally; and Sect. 5 concludes the best performance of boosted pierce resonator circuit implementation.

2 MEMS SAW resonator

Surface acoustic wave (SAW) devices can be implemented as the frequency determining element or as filter in RF applications (Karim et al. 2012). Advancement of manufacturing techniques in the CMOS technology now lures the MEMS SAW resonator to be applied using CMOS fabrication techniques (Uranga et al. 2015). The performance of the resonators is measured based on their Q factor. The higher the Q, the better the signal received by the transceiver. As reported in Chengjie et al. (2010), current MEMS resonators have shown great performance with measured Q factors > 1000 and can operated in GHz frequency range. Conventional SAW devices have been widely implemented as filters and oscillators with operation frequency higher than quartz crystal. SAW devices offer certain advantages such as high Q, low spurious tone, which results in excellent phase noise and low power (Otis 2002).

Monolithic CMOS-MEMS integration provides robust platform to realize low power and low cost mass production for a single chip solution. The CMOS MEMS SAW resonator is using a mixed of CMOS layers with a piezo-electric material on top. The zinc oxide SAW resonator implemented in standard CMOS ($0.6 \mu m$) and RF-CMOS ($0.18 \mu m$) were first introduced in Nordin and Zaghloul (2008). The resonance frequencies of CMOS MEMS SAW resonator varies from 600 MHz to 3.12 GHz while the Q factor ranges from 44 to 285 (Nordin and Zaghloul 2008).

Progression of implementation of CMOS SAW resonators in standard CMOS using different piezoelectric thin film such as aluminium nitride are presented. Eight different design of the CMOS-MEMS SAW resonator was fabricated. The wavelengths are varied to produce resonant frequencies of 0.9–1.4 GHz. The microscope image of eight resonators at different wavelengths is shown in Fig. 1. S₂₁ measurement was carried out to measure series resonance frequency (f_s), parallel resonance frequency (f_p) and insertion loss. Measurement results revealed the resonance frequencies are 1.40 and 1.0 GHz for CMOS SAW resonator implemented on ZnO and AlN thin film respectively as shown in Fig. 2.

The CMOS SAW resonator must first be extracted into its equivalent circuit model before the CMOS oscillator topology can be designed. The accuracy of the extracted parameters is very crucial since it determines the performance of the oscillator. Equivalent circuit model represents the resonator as a lumped-element circuit in electrical domain. The parameters of the equivalent circuit model are related to the physics and



Fig. 1 Device under test (DUT)-CMOS-MEMS SAW resonator

Fig. 2 Frequency vs. insertion loss for a ZnO CMOS MEMS SAW resonator b AlN CMOS MEMS SAW resonator fabrication process of the resonator. Figure 3 is the fitted equivalent circuit model for SAW resonator. The circuit comprised of motional resistance Rm, motional inductance Lm, motional capacitance Cm and static capacitance Cf. Rs1, Rs2, Rp1, Rp2, Cox1, Cox2, Ct1 and Ct2 are the parasitic resistance and capacitance. The values of each components are shown in Table 1. Resonant frequency is at 1.40 GHz with insertion loss of - 65.1 dB.

3 Boosted pierce circuit design

An oscillator generates oscillation without any external input. The basic oscillator system comprises of amplifier circuit and frequency determining network. The system is illustrated in Fig. 4. The frequency determining network can either be the resonator or the LC or RC circuit. In this case, the frequency determining network is the MEMS SAW resonator. The sustaining circuit or the amplifier



| ······································ | | | | | | | | | | | |
|--|-----------------------|------------------------|------------------------|--|------------------------|--|---|---|---|---|--|
| Resonator | R _m (Ω) | L _m (µH) | C _m (fF) | $\begin{array}{c} R_{\rm f} \\ (\Omega) \end{array}$ | C _f (pF) | $\begin{array}{c} R_{s1} \ (\Omega) \end{array}$ | $\begin{array}{c} R_{s2} \\ (\Omega) \end{array}$ | $\begin{array}{c} R_{p1} \\ (\Omega) \end{array}$ | $\begin{array}{c} R_{P2} \\ (\Omega) \end{array}$ | $\begin{array}{c} C_{ox1}+C_{t1} \\ (pF) \end{array}$ | $\begin{array}{c} C_{ox2}+C_{t2}\\ (pF) \end{array}$ |
| ZnO CMOS SAW resonator | 512 | 2.13 | 6.05 | 91.8 | 29.58 | 493 | 412 | 22.1 | 19.4 | 2.36 | 2.72 |
| AlN CMOS SAW resonator | 35 | 4.0 | 6.10 | 50 | 62.0 | 150 | 500 | 85 | 2 | 1000 | 5000 |

Table 1 Extracted equivalent circuit parameters for ZnO and AlN CMOS MEMS SAW resonator



Fig. 3 Modified equivalent circuit modeling parameters for CMOS MEMS SAW resonators

circuit enables its own noise to enlarge and develop into a periodic signal.

Barkhausen stability criterion highlights that if A is the gain of the amplifying element in the circuit and $\beta(j\omega)$ is the transfer function of the feedback path, so βA is the loop gain around the feedback loop of the circuit, the circuit will retain the steady-state oscillations only at frequencies which the loop gain is equal to unity and the phase shift around the loop is zero. In this work, the S-parameter two-port model of the resonator has been adopted for better accuracy. Better accuracy is obtained by direct usage of S-parameters of the resonator. The equivalent circuit model usually may give errors when fitting the equivalent circuit to the measured results.

Pierce oscillator circuits are popular as MEMS oscillator circuits due to their low-noise and low power characteristics and the simplicity of the system. The enhanced transistors are usually biased in the weak inversion region in order to maximize the transconductance, to maximize the gain $(A(j\omega))$ and to deal the loss of the MEMS resonator as well.

As shown in Fig. 2, the insertion losses of the CMOS MEMS SAW resonator is extremely high; ~ 65 dB while its Q factor is low and is less than 800. A simple single transistor Pierce oscillator will not be sufficient to sustain



Fig. 4 Basic oscillator block diagram

oscillation. To overcome the matter, a boosted pierce topology was suggested. This entails the usage of cascode or stacked transistors to provide the gain boost. Two threestage amplifiers were connected to supply sufficient gain. The configuration is designed as such in order to reimburse with the insertion loss of SAW without having voltage overdrive consideration limitation.

The proposed circuit are built with an active cascade amplifier and a two-stage cascode of amplifier with separated supply voltages in order to compensate with higher insertion loss SAW. The schematic of the boosted pierce oscillator circuit is shown in Fig. 5.

The 1st stage amplifier consists of three pairs of transistors; N1–N3 and P1–P3 together with three resistors, R1–R3. The resistors R1, R2 and R3 play the role as a feedback resistor to linearize the inverter of combination P1/N1, P2/N2 and P3/N3. The value of the resistors implemented are sufficient to bias the inverters in the linear region to produce a high gain at the 1st inverting amplifier. The 2nd stage amplifier is also called as a three stage of amplifier. In this stage, active resistors Nfb1, Nfb2 and Nfb3 were used as large bias resistors to the gate of N4, N5 and N6. The N6 transistor offers the critical transconductance for oscillation and is biased by P6. This amplifier operates in weak inversion region for the high transconductance gm.

The regulated cascode output circuit has been implemented using two stacked NMOS transistors; N8, N7 and R4. The key function of the booster is to enhance gm for N8, which further

Fig. 5 Boosted pierce oscillator circuit



increases the output resistance and the gain of the amplifier. This is done by inaugurating a push–pull operation between source and gate voltage of N8 through the insertion of 1st and 2nd stages of amplifier. The drain current at N8 is 321 μ A with the parameter of transistor N8 and N7 is 10/0.13 μ m. The design parameters of the other transistors were detailed in Table 2. The circuit was implemented using Silterra CMOS 0.13 μ m technology and simulated using Spectre.

4 Simulation results

Figure 6 shows the physical layout design of pierce oscillator circuit with GSG pad connection. There are two inputs voltages which is VDD1 for 1 V and VDD2 for 1.4 V with boosted circuit. The CMOS SAW resonator will be bonded to this pierce oscillator circuit at the input (IN) and output (OUT) of the oscillator circuit. Thus the bondpads are designed to have very low parasitic capacitance so that they will not overload the oscillator.

Figure 7 illustrates the transient output simulation for MEMS SAW oscillator. The oscillation frequency generated using closed loop simulation was roughly at 1.3 GHz with a voltage swing of about 800 mV (approximately

| Table 2 | Boosted | pierce | oscill | a- |
|-----------|----------|--------|--------|----|
| tor circu | it param | eters | | |

| 1 - | Transistor | Size |
|------------|------------------------------------|----------|
| | P ₁ –P ₃ | 120/0.13 |
| | $P_4 - P_6$ | 3/0.13 |
| | N ₁ -N ₃ | 10/0.13 |
| | N ₄ -N ₆ | 64/0.13 |
| | N ₇ –N ₈ | 10/0.13 |
| | N _{fb1} -N _{fb3} | 4/0.13 |
| | R_1-R_3 | 5 ΜΩ |
| | R_4 | 1 kΩ |
| | | |

between 0.92 and 0.15 V) as shown in Fig. 8. The phase noise is—92.63 dBc/Hz at 1 MHz as shown in Fig. 9. The simulated admittance plots (S21) for MEMS SAW with insertion loss of approximately - 65 dB.

Table 3 indicates the performance comparison of the existing MEMS based oscillators with the MEMS SAW oscillator. The oscillator in this work has demonstrated comparable power consumption with 2.4 V DC supply. Higher losses of SAW resonator too is not a hindrance to achieve comparable phase noise performance if the sustaining amplifier circuit is properly designed. Furthermore the oscillation frequency of oscillator produce in this work is in GHz range compared with the existing MEMS based oscillator.

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| Table 3 Performance compa | rison of | CMOS-MEMS | oscillators |
|---------------------------|----------|-----------|-------------|
|---------------------------|----------|-----------|-------------|

| | Lavasani et al. (2015) | Chengjie et al. (2011) | Seth et al. (2012) | This work |
|-----------------------|---|---|---|---|
| Process | 0.5 µm | 0.35 μm | 0.35 μm | 0.13 μm |
| V _{dd} (V) | 2.5 | 2.5 | - | 2.4 |
| Phase noise | — 112 dBc/Hz/103 dBc/Hz @1- KHz | – 120 dBc/Hz @ 1 MHz | — 110 dBc/Hz @ 1 MHz | – 92.63 dBc/Hz @ 1 MHz |
| Resonator losses | — 14 dB | – 30 dB @ 50 V | + 0.5 dB @ 75 V | - 65 dB |
| Power consumed (mW) | 3.8 | 1.3 | 1.6 | 1.52 |
| Oscillation frequency | 35.5/175 MHz | 1.2 MHz | 1.2 MHz | 1.3 GHz |

Fig. 8 Simulated oscillation of SAW resonator





Phase Noise; dBc/Hz, Relative Harmonic = 1



5 Conclusion

The simulation of pierce oscillator circuit with boosted gain to compensate the high insertion loss of the MEMS SAW resonator has been carried out. The circuit was designed and optimized based on touchstone S_2P measurement results file of the MEMS SAW resonator. Direct usage of the S_{21} measurement results versus the conventional equivalent circuit simulations provides a more accurate prediction of the oscillator performance before fabrication. The 1.3 GHz oscillator shown – 92.63 dBc/Hz at 1 MHz offset and is comparable with existing MEMS based oscillator. The oscillator core consumes 1.52 mW DC power.

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