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**CNTFET inverter: A high voltage gain logic gate** (Conference Paper)

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## Abstract

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Conventional CMOS technology provides a lot of opportunities in the field of electronics device. But presently, carbon nanotube field effect transistor (CNTFET) is a new technology for the application in the field of electronic device. Due to the limitation of the size of CMOS, CNTFETs are the promising substitute due to its nano scale size. CNTFET also shows the high stability, low power circuit design, high signal to noise margin (SNM) and high gain in the circuit design. A novel design of CNTFET based inverter with an optimum chiral vector is proposed in this paper. PSPICE platform is used to model and simulation this CNTFET inverter circuit. The proposed CNTFET inverter circuit is investigated based on noise margin characteristics. A maximum voltage gain of 45dB is observed from NCNTFET of the inverter and a high noise margin of 400mV and a low noise margin of 309mV are achieved from the proposed inverters. This approach is a useful technique for fabricating integrated logic devices and circuits based on CNTFETs.  
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## Author keywords

CNTFET gain inverter noise margin

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