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Hardware realization of an efficient fetal QRS complex detection algorithm (Article)

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Abstract

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An algorithm has been developed for the simultaneous measurement of the fetal and maternal heart rates from the maternal abdominal electrocardiogram during pregnancy and labor for fetal monitoring. The algorithm is based on cross-correlation, adaptive thresholding and statistical properties in the time domain. The algorithm was initially developed and simulated in Visual C++. Once the functionality is verified, it is then converted in VHDL - hardware description language for FPGA implementation. The design is synthesized and fitted into Altera's Stratix EP1S10 using the Quartus II platform because of its enhanced DSP capability. Test case results showed an error percentage of around ±0.3% and ±0.5% for the detection of maternal and fetal heart rate respectively. The system is capable to run at a maximum clock frequency of 48.56MHz, and consumed 9633 logic elements, 101616 memory space and 4 units of DSP blocks.

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Author keywords

Electrocardiogram Fetal heart rate FPGA VHDL

Indexed keywords

Engineering controlled terms: Adaptive algorithms Computer simulation Correlation methods Electrocardiography Fetal monitoring Time domain analysis

Engineering uncontrolled terms: Adaptive thresholding Cross-correlation Fetal heart rate Maternal heart rates

Engineering main heading: Algorithmic languages

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