

SELECTED TOPICS IN ADVANCED ELECTRONICS

Edited by
Khalid A. S. Al-Khateeb



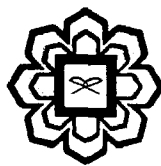
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CHAPTER 29

MODELING CMOS WAFER PRODUCTION LINE USING PROMODEL SOFTWARE

By

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Synopsis

This chapter presents and discusses a model for an actual CMOS wafer production line. The performance of the production flow is evaluated using simulation technique to optimize the yield and the time cycle. The simulation model is based on ProModelTM software. It incorporates various manufacturing activities. The validation of the model is based on conducting a series of tests. The theoretical cycle time to process a wafer lot in the system under test is 13.07 days. The initial configuration assumes that all equipments have a queue capacity of one wafer cassette. Such configuration did not prove to be practical. Then a queue size of five wafer cassette was applied to all stages in the production line. The test parameters include; walking speed of operator, cross training, shift work schedule 48 min. break for an 8-hour (480mintues) shift, and equipment operation 92% of the simulation time. Optimization for a 24hour, 7days a week shift revealed that inter-arrival time is 40hours, which is a determining factor production line performance, provided that the overall production cycle time and system work in progress (WIP) level remain within an acceptable range, and assuming a constant number of operators. Simulation for duration of one year the model yields an overall operator utilization of 42% an average WIP 12.3 wafer lots, an average cycle time of 19.92 days and a weekly throughput of five wafer lots. Added to the simulation programme, animation was made to illustrate the production paths.