

# SELECTED TOPICS IN ADVANCED ELECTRONICS

Edited by  
Khalid A. S. Al-Khateeb



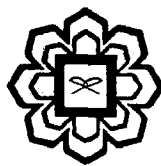
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**ADVANCED ELECTRONICS**

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# CHAPTER 31

## ELECTRONIC DESIGN AUTOMATION TOOLS

By

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### Synopsis

Electronic Design Automation (EDA) tools are linked with the ASIC design flow. Synopsys, being one of the largest vendors of EDA tools in the industry, is taken as an example. One of its best-known tool is Design Compiler (DC), a logic-synthesis tool. Synopsys offers a wide range of other tools used in the design of the Application-Specific Integrated Circuit (ASIC). The aim is to provide the readers with a general knowledge about Synopsys as an EDA tool. Products include logic synthesis, behavioral synthesis, place and route, HDL (SystemC Systemverilog/Verilog and VHDL), static timing analysis, formal verification, simulators as well as transistor-level circuit simulation. This chapter is considered as a quick reference for the tools included in Synopsys Electronic Design Automation (EDA) package. It presents a brief description about VCS, Design Compiler, Designware library, Formality, Primitime, IC Compiler, Hercules, StarRC, TetraMAX.

### 1 Introduction

VCS is a high-performance, high-capacity Verilog simulator that incorporates advanced, high-level abstraction verification technologies into a single open native platform. VCS is a compiled code simulator. It enables the designer to analyze, compile, and simulate Verilog, SystemVerilog, OpenVera and SystemC design descriptions. It also provides a set of simulation and debugging features to validate the design. These features provide capabilities for source-level debugging and simulation