

Selected Readings in
**COMPUTING AND
TELECOMMUNICATIONS**

Editors
Mira Kartiwi
Teddy Surya Gunawan
Aisha Hassan Abdalla Hashim



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18. IMPLEMENTATION OF CAPACITANCE OF VOLTAGE CONVERTER FOR CAPACITIVE TRANSDUCERS

A.H.M. Zahirul Alam and Nur Fadhila bt. Che Halim

ABSTRACT

Implementation of Capacitance to Voltage Converter for Capacitive Transducer is another new design of Capacitance to Voltage Converter (CVC) circuit. This CVC has several advantages over other CVC circuit such as low power consumption, high precision, wider range of detection and low cost material. The main objective of this CVC is to encounter the problem facing by other available CVC circuit such as limited range of detection, high power dissipation due to high power consumption and low precision. Switching mechanism is the main feature introduce in the new CVC design. Switch is replace by NMOS in this design and the two phase non overlapping clock is used to control the NMOS that act as a switch in the CVC. The CVC circuit is simulated using PSPICE and the result is compared between simulation and experimental. The result show that the relationship between output voltage due to variation in capacitance value have same pattern for both simulation and experiment eventhough the difference is quite large due to the errors in hardware implementation.

18.1 INTRODUCTION

Capacitance to Voltage Converter (CVC) is used in many systems that required capacitor to act as a sensing device. Since capacitive sensors are becoming more and more popular, many methods (Ignjatovic, et. al., 2005; Arfah, 2011) have been introduced which deal with the conversion of capacitance values into a voltage. In CVC, variation in capacitance value is