INTERFACING ELECTRONIC FOR MEASUREMENT, SIGNAL PROCESSING AND WIRELESS COMMUNICATION

Edited by

Sheroz Khan, International Islamic University Malaysia

AHM Zahirul Alam, International Islamic University Malaysia

Anis Nurashikin Nordin, International Islamic University Malaysia

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INTERNATIONAL ISLAMIC UNIVERSITY MALAYSIA

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Chapter 26

MVL ADC DESIGN AND SIMULATION

SOHELI FARHANA, AHM ZAHIRUL ALAM, SHEROZ KHAN

26.1. INTRODUCTION

The design and simulation of a higher radix (MVL) analog-to-digital converter (ADC) circuit is presented in this chapter. The ADC generates multi-valued logic outputs rather than the conventional binary output system. The design implements pipeline ADC architecture and is simulated using the model parameters for a standard 0.13μm CMOS process. The performance analysis of the design shows desirable qualities in terms of response, low power consumption, and a sampling rate of 500kHz at a supply voltage of 1.3V. The ADC design is suitable for the needs of mixed-signal integrated circuit design and can be implemented as a conversion circuit for systems based on multiple-valued logic design.

26.2. PROPOSED ADC ARCHITECTURE

The proposed design implements current mode pipeline ADC architecture to convert analog signals into quaternary logic (radix-4) values. The configuration for a 4-bit resolution converter of the design is shown in Fig. 26.1. The conversion process involves using cascaded levels of comparator cells with the output of each block representing each bit of the digitized output. Hence the possible number of cascaded levels defines the resolution of the converter. The inputs to the comparator cell are the analog input current to be digitized, Iin and the reference current, IRef. The reference current used here is equivalent to the current value of a single logic level, ILogic. The comparator block produces an output of discretized current levels IOut which are multiples of the logic value current, ILogic. The current output level, IOut depends on how large the input current, Iin is in comparison to multiples of the reference current IRef. The comparator cell is also designed to produce an output current, IDiff which is the difference between the analog input current Iin and the output current level IOut. The current difference output, IDiff is used to facilitating the cascading of comparator cells. For IDiff to be used at the next input stage it however has to be scaled by a factor of four since the whole current input range has been discritized to four output levels. So the inputs to the next comparator cell will be four times IDiff in place of the analog input current, Iin and the reference current IRef will be retained from the preceding stage. The whole process is repeated and hence the input currents for each successive stage i of the comparator cell with the reference current, IRefi and the input current Iini is defined by the relation:

$$Iin_i = 4*(Iin_{i-1} - IOut_{i-1}) \quad (1)$$