ADVANCES IN MATERIALS ENGINEERING

Volume 2

Edited By:
Md Abdul Maleque
Iskandar Idris Yaacob
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IIUM PRESS
INTERNATIONAL ISLAMIC UNIVERSITY MALAYSIA

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Published by:
IIUM Press
International Islamic University Malaysia

First Edition, 2011

Perpustakaan Negara Malaysia Cataloguing-in-Publication Data

Md Abdul Maleque, Iskandar Idris Yaacob & Zahurin Halim: Advances in Materials Engineering

ISBN: 978-967-418-168-0

Member of Majlis Penerbitan Ilmiah Malaysia – MAPIM
(Malaysian Scholarly Publishing Council)

PRINTED BY:
IIUM PRINTING SDN.BHD.
NO. 1, JALAN INDUSTRI BATU CAVES 1/3
TAMAN PERINDUSTRIAN BATU CAVES
BATU CAVES CENTRE POINT
68100 BATU CAVES
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Chapter 025

Stress Analysis of Backend Metallization

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Keywords: VLSI, Fluorine-doped silicate glass (FSG), Silicon-rich oxide (SRO), DF SRO, SF SRO wafer bow.

Abstract. The backend structures of advanced VLSI (Very-Large Scale Integration) devices have become increasingly complex because of the need to combine several types of dielectric and metal layers in order to enhance device performance and/or reliability. For example, the inter-metal dielectric (IMD) stack of an aluminum-metallization device may consist of high density plasma (HDP) fluorine-doped silicate glass (FSG) for gap fill and RC-delay minimization, plus a silicon-rich oxide (SRO) cap to prevent aluminum attack from fluorine out-diffusion. Depending on the interplay between the tensile stress of the aluminum, and the typically compressive stress of the dielectric stack, the wafer may develop a large bowl of either positive or negative sign. A large positive bow may negatively impact wafer handling during processing steps that use vacuum chucking, and can also lead to excessive edge polishing during tungsten and oxide chemical–mechanical planarization (CMP) steps. This paper presents a methodology to reduce final wafer bow from ~+40 to ~-10 micron by a careful selection of SRO deposition conditions to achieve a stress value that results in flatter wafers.

Introduction

Modern microelectronic device sizes have been scaled down to increase transistor speed and maximize the integration achievable on a die. The reliability of IC's strongly depends on the thermal stresses that develop in the multilevel interconnects, due to potentially large differences in the thermal expansion between metal lines and surrounding environment as the entire structure undergoes thermal excursions during processing and service [1]. Figure 25.1 shows a schematic diagram of a typical CMOS IC (complementary metal oxide semiconductor integrated circuit) with three levels of aluminum metallization.

FSG is being adopted in microelectronic manufacturing due to its low dielectric constant and stable gap-filling ability [2]. It is well known that fluorine is an active atom, which reacts easily with other elements [2], and thus, fluorine might attack aluminum metal. In order to avoid fluorine out diffusion, FSG is typically capped with a SRO film, in which the excess silicon atoms bind with and tie up the fluorine. In this study, SRO was employed as the cap for FSG. The FSG/SRO stack is referred to as IMD (Inter-Metal Dielectric) layer. The SRO films are prepared by plasma enhanced chemical vapor deposition (PECVD) on a Novellus Sequel chamber, using dual frequency RF power [3]. On this tool, the combination of high (13.56 MHz) and low (300-400 KHz) frequency RF provides control of film stress and can improve step coverage, film density, chemical composition and film stability. A graph of SRO stress vs. %LF RF power is shown in Figure 25.2. As the LF RF component of