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REVIEW PAPER

Leakage Current Mechanisms in Silicon Carbide MOSFETs - A Review

Tamana Baba[1] · Nurul Fadzlin Hasbullah[1] · Norazlina Saidin[1] · Naseeb Ahmad Siddiqui[2] · Abdullah Üzüm[3] · Mehmet Turhal[3]

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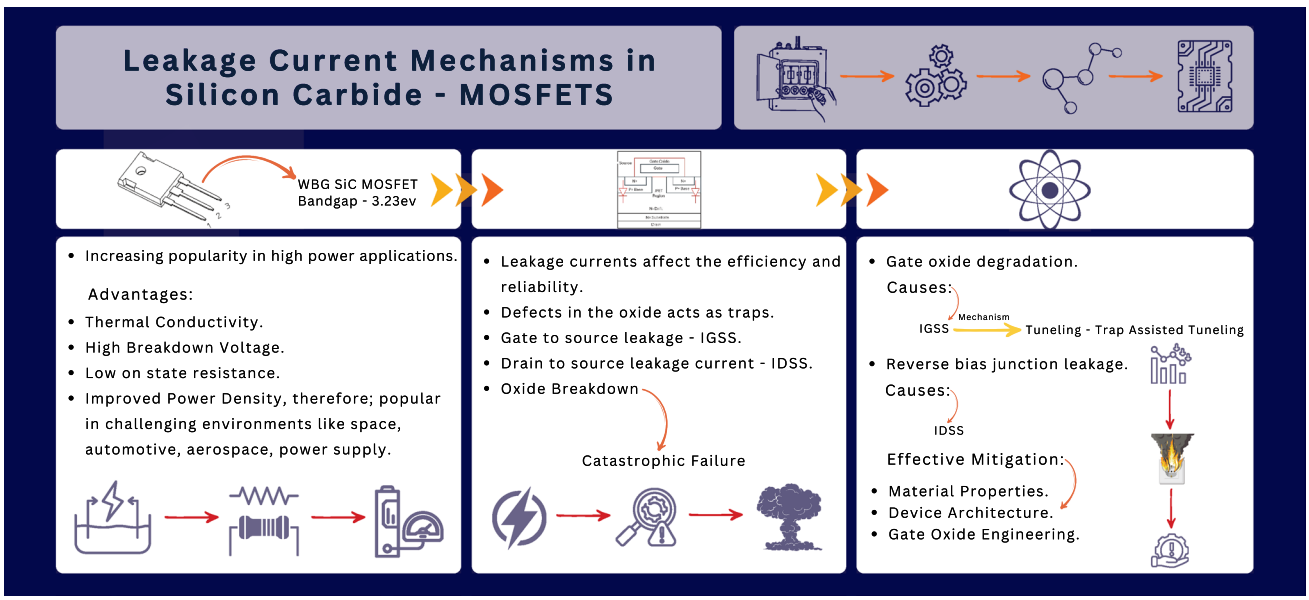
Abstract

MOSFETs are integral components in modern electronics, renowned for their efficiency and performance. However, leakage currents, including drain-source (I_{DSS}) and gate-source (I_{GSS}) currents, pose significant challenges to device reliability and overall system efficiency, leading to issues such as increased power loss, thermal stress, and reduced lifespan of devices. This review delves into the mechanisms underlying leakage currents in SiC MOSFETs, a promising technology for high-power applications. The key factors contributing to leakage, such as gate oxide degradation, material properties, and device architecture, have been identified by examining the research conducted over the past few years. Understanding the leakage current mechanisms is crucial for developing effective mitigation strategies and optimizing SiC MOSFET performance. This review concludes by summarizing key findings and highlighting the importance of ongoing research.

Graphical Abstract



Keywords Gate leakage · Junctions · Leakage currents · MOSFET · Silicon carbide (SiC) · Tunneling

✉ Nurul Fadzlin Hasbullah
nfadzlinh@iium.edu.my

[1] Department of Electrical and Computer Engineering, Kulliyyah of Engineering, International Islamic University Malaysia, Kaula Lumpur, Malaysia

[2] National University of Singapore, Queenstown, Singapore

[3] Department of Electrical and Electronics Engineering, Faculty of Engineering, Karadeniz Technical University, Trabzon, Türkiye, Turkey

1 Introduction

Metal-oxide-semiconductor field-effect Transistors (MOSFETs) serve as the principal constituent of contemporary electronic systems, underpinning the functionality of devices ranging from simple calculators to sophisticated supercomputers [1, 2]. Their unparalleled capacity to amplify and switch electronic signals with remarkable efficiency and speed has propelled advancements in computing, telecommunications, and consumer electronics [3, 4]. Characterized by their high input impedance and rapid switching capabilities, MOSFETs have revolutionized circuit design and enabled the miniaturization of electronic components [5, 6].

In recent years, the limitations of silicon (Si) based MOSFETs have driven the search for alternative materials [7, 8]. Among these, silicon carbide (SiC), a wide-bandgap semiconductor, has come out as an encouraging option for high-power electronics. SiC MOSFETs offer significant advantages, including higher breakdown voltage, lower on-resistance, and better thermal conductivity compared to their Si counterparts [9]. These characteristics result in improved power density, reduced energy losses, and enhanced system reliability. Consequently, SiC MOSFETs are increasingly being used in demanding applications such as electric vehicles, space electronics, aviation, and industrial motor drives [10, 11].

A clear example of the advantages of SiC MOSFETs is their superior performance in high-power, high-temperature environments compared to Si-based devices. SiC MOSFETs exhibit much lower on-resistance, higher breakdown voltages, and greater thermal stability, making them well-suited for such applications [12]. Shenai et al. showed that at high operating temperatures, a SiC device has considerably higher on-state conductance and smaller off-state leakage current than Si devices. This resulted in a decrease in the power dissipated in the active device area and, thus, the Sic devices showed desirable performance even for very-high junction temperatures [13]. Similarly, C. Unger and M. Pfost investigated thermal stability by means of high-temperature characterization, measurements up to destruction, and electro-thermal simulations. It was shown that the temperature dependence of the threshold voltage V_{th} diminishes at high temperatures, which leads to thermally stable operation at elevated temperatures of SiC-based MOSFETS. On the contrary, the nonuniform current distribution and the formation of hot spots can still be a concern at low V_{GS} [14]. However, Z. Li et al. showed that prolonged exposure conditions of SiC MOSFETs to high temperatures may induce stress on the SiO_2/SiC interface, which leads to a decrease in electron mobility and thus reduces the transconductance and drain current [15].

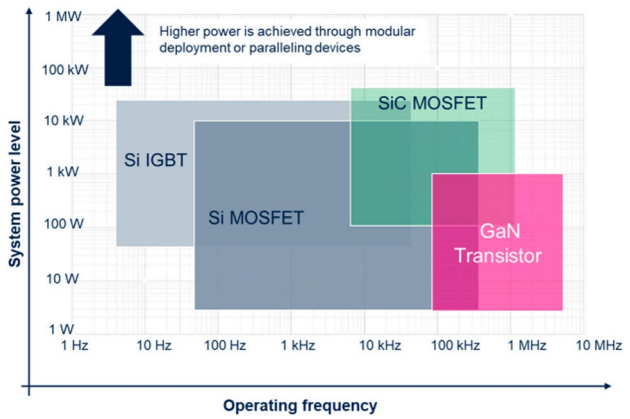


Fig. 1 Power technologies at different frequencies [16]

Figure 1 highlights the key power technologies on a power-frequency diagram, showing that wide-bandgap (WBG) materials like SiC and GaN have been developed due to their lower on-resistance and ability to operate at higher frequencies, which significantly reduces losses and improves system efficiency. While gallium nitride (GaN) is mostly used in the 100 V to 900 V range, SiC excels at higher voltages, exceeding 650 V and even surpassing 2000 V. This broader voltage range emphasizes the superiority of SiC over Si in power electronics, where high voltage and efficiency are essential. SiC MOSFETs are thus enabling more compact and efficient designs in power converters and motor drives, outperforming their Si equivalents in both performance and reliability [16].

However, leakage currents in MOSFETs, although typically small, can substantially affect the efficiency and dependability of devices [17, 18]. These currents are unintended flows of charge that occur even when the device is in an off-state (I_{DSS}) or through the gate oxide (I_{GSS}) [19]. Leakage currents can lead to a variety of problems, including increased power dissipation, which reduces the overall efficiency of electronic systems. Moreover, these currents contribute to elevated operating temperatures, causing thermal stress that can accelerate device aging and degradation. Over time, the higher temperatures may cause the breakdown of the gate oxide, exacerbating leakage and potentially causing catastrophic device failure. Furthermore, leakage currents reduce the switching speed of MOSFETs, negatively affecting the dynamic performance of circuits. In applications where safety is paramount, such as in aerospace and automotive electronics, uncontrolled leakage can compromise system reliability and stability, making it a crucial factor to address in device design and material selection. In SiC MOSFETs, managing leakage currents is critical because of the material's intrinsic properties and the high voltages at which these devices operate. Understanding the mechanisms behind I_{DSS} and I_{GSS} is paramount for

maximizing device efficiency and ensuring long-term reliability [20].

This review comes up with a detailed examination of the fundamentals of SiC MOSFETs, emphasizing their advantages over traditional Si-based MOSFETs. A comprehensive analysis of leakage current mechanisms is central to this paper, with a particular focus on I_{DSS} (drain-source leakage current) and I_{GSS} (gate-source leakage current). I_{DSS} is highlighted for its significant role in off-state power losses, while I_{GSS} is examined in relation to the risk of gate oxide breakdown, a critical failure mode for SiC devices operating at high voltages.

This paper makes a substantial contribution to the existing body of knowledge on leakage currents in MOSFETs, with a focus on SiC technologies. It systematically explores the underlying physical mechanisms that contribute to these leakage currents, providing a thorough review of recent research. Factors influencing I_{DSS} and I_{GSS} are discussed in depth, including material properties, device architecture, and environmental conditions. The review also addresses the broader impact of leakage currents on MOSFET performance, particularly in terms of device efficiency, thermal management, and long-term reliability. Mitigation strategies to minimize these leakage currents, such as improvements in gate oxide integrity and optimized device designs, are presented as well. Additionally, future research directions are outlined, particularly in the context of advancing SiC MOSFET technologies for high-power and harsh-environment applications. This review fills a critical gap in the literature by offering a focused discussion on leakage current mechanisms in SiC MOSFETs, which is often overlooked in broader reviews [12, 21–23]. By addressing I_{DSS} and I_{GSS} comprehensively, this paper underscores the importance of controlling leakage currents to promise the optimal performance and reliability of SiC-based devices.

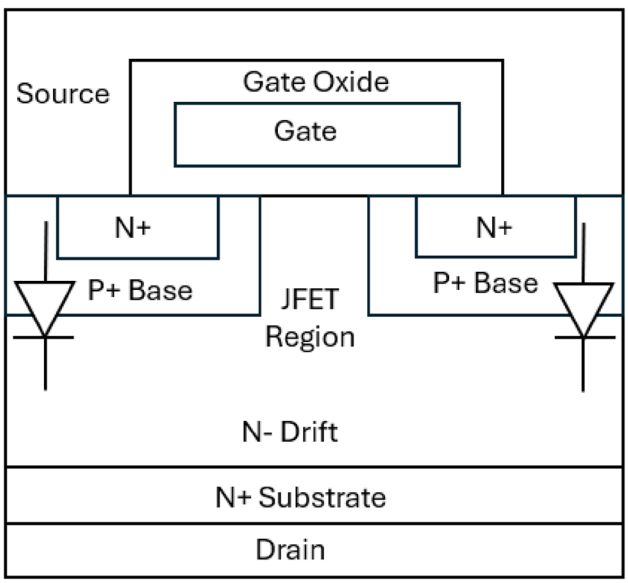


Fig. 2 Planar structure of an enhanced n-channel SiC MOSFET [27]

The rest of the paper is organized as follows: Sect. 2 presents an overview of the basics of a SiC MOSFET device and the merits of a SiC MOSFET over the traditional Si counterpart. Section 3 presents a detailed discussion of the mechanisms of leakage currents in SiC MOSFET. All significant mechanisms contributing to I_{DSS} and I_{GSS} have been discussed in detail. Section 3.2.2 presents a discussion on the factors affecting the leakage currents in MOSFET. A brief discussion on the radiation-induced leakage current and its effects on the working of MOSFET is presented in Sect. 4. The strategies that can be employed for the mitigation of leakage current in MOSFET are presented in Sect. 5. Section 6 presents the future trends in this research. Finally, Sect. 7 concludes the review paper.

2 Fundamentals and Basic Working Principle of a SiC MOSFET

2.1 SiC MOSFET

SiC MOSFETs are available in various forms, classified by their conductive channel as either n-channel or p-channel. They also come in two main types: enhancement and depletion, based on their conduction mode [24]. Enhancement-type MOSFETs remain off when the gate-to-source voltage (V_{GS}) is zero, requiring a positive voltage (n-channel) or negative voltage (p-channel) to turn on and allow current flow by attracting charge carriers into the channel region [25]. These MOSFETs are commonly used in digital circuits due to their low power consumption when inactive. Depletion-type MOSFETs, on the other hand, are normally on when V_{GS} is zero, with a voltage opposite to the channel type required to turn them off. A negative gate voltage reduces the current in n-channel depletion MOSFETs, while a positive voltage does the same for p-channel versions. These MOSFETs are more often used in analog circuits where a normally-on switch is required [26].

Figure 2 depicts the structure of an n-channel enhanced SiC MOSFET by Roma Semiconductor, featuring vertical conduction that improves strength, electrical resistance, and avalanche energy, distinguishing it from traditional Si MOSFETs by having the drain at the bottom to create a vertical current path [27].

The SiC MOSFET is fabricated using ion implantation and epitaxial growth to precisely form the source (N+), base (P), and drift (N-) regions. When a positive gate voltage is supplied, an electric field forms in the oxide layer, attracting electrons to the junction between the base and oxide layers and creating a short channel for conduction. This increases

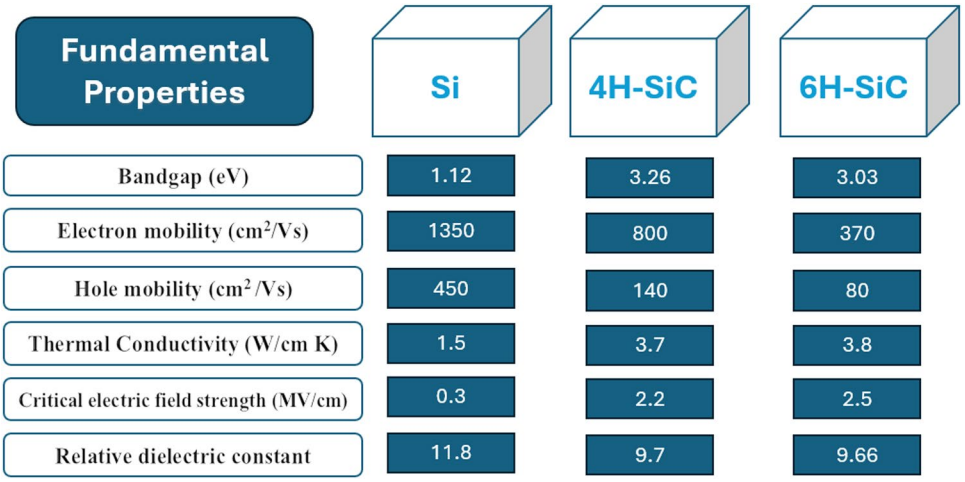


Fig. 3 Comparison between the properties of Si and SiC [32]

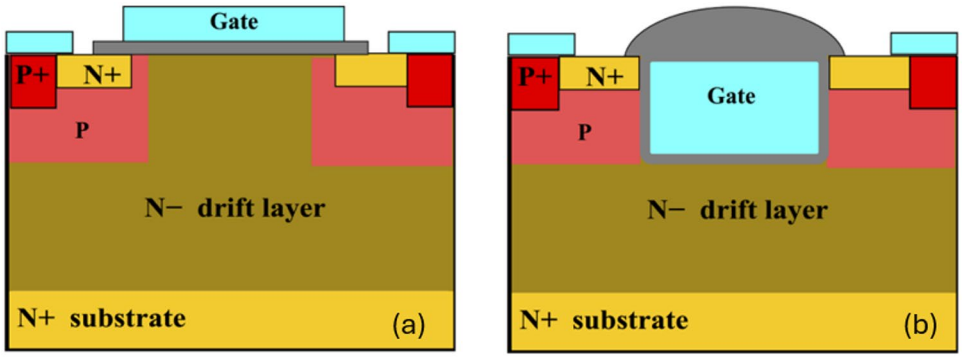


Fig. 4 Cross-sectional views of (**a**) Planar Gate SiC MOSFET and (**b**) Trench Gate SiC MOSFET structures [33]

the device's current-carrying capacity and drain current. The high electron mobility enables fast switching speeds. The P+base and N- drift regions form a pn junction, acting as a body diode. The source (N+), base (P+), and drift region (N-) create a triode structure, while the gate oxide layer insulates the gate from the base, improving stability. SiC's high breakdown field strength allows the drift region to remain resistive even with a thinner design [28].

2.2 Si vs. SiC MOSFET

Both Si and SiC are extensively utilized in power electronics, but they exhibit significant differences due to the distinguishable material properties of Si and SiC. SiC MOSFETs have several advantages over their Si counterparts, primarily due to SiC's wider bandgap, higher thermal conductivity, and superior electric field strength. These properties allow SiC MOSFETs to work at higher voltages, temperatures, and switching frequencies with lower conduction and switching losses [29]. Specifically, SiC MOSFETs can handle higher breakdown voltages, making them ideal for high-power applications. Besides, the higher thermal conductivity of SiC allows for better heat dissipation, reducing the need for complex cooling systems. The faster switching speed of SiC MOSFETs results in more efficient and compact power converters. However, SiC devices are generally more expensive than Si devices owing to the higher cost of SiC substrates and manufacturing processes [30]. Despite this, the performance benefits of SiC MOSFETs often justify the higher cost in applications requiring high efficiency and reliability. SiC can adopt various crystalline structures based on its stacking order, a phenomenon known as polytypism, with each structure referred to as a polytype. Consequently, SiC is classified as a polytypic material with approximately 250 distinct polytypes. The most commonly utilized polytypes are 6 H-SiC and 4 H-SiC, as they can be manufactured into large wafers and are readily available for device fabrication. Figure 3 compares the properties of Si and SiC [31].

2.3 SiC-Based MOSFET Structures

SiC MOSFETs are available in several structural variants that significantly influence their behavior. Figure 4 illustrates the two most common vertical SiC MOSFET structures: the planar gate MOSFET and the trench gate MOSFET. Both structures employ a vertical current flow through the N−drift layer and N+substrate to achieve high blocking voltage capability, but they differ significantly in

channel formation and gate oxide geometry, which directly influences leakage current behavior [33].

In the planar design, the gate electrode is formed on a flat surface over the P-well region, where the inversion channel develops laterally under the gate oxide. The simpler planar geometry results in a more uniform electric field distribution across the gate oxide. Gate leakage current I_{GSS} in planar SiC MOSFETs is primarily governed by the quality of the gate oxide and the interface state density at the SiC/SiO_2 interface. While planar structures are generally easier to fabricate with reliable oxide characteristics, they typically have lower channel density, leading to higher specific on-resistance compared to trench designs [34].

In contrast, the trench gate MOSFET features a vertically etched trench filled with gate material and lined by gate oxide. The inversion channel forms along the vertical sidewalls of the trench. This design significantly increases channel density, reducing specific on-resistance. However, the trench geometry creates regions of enhanced electric field concentration, especially at the trench corners, making the gate oxide more susceptible to stress-induced leakage and reliability degradation. Gate leakage in trench designs tends to be higher if oxide processing is not carefully optimized, requiring advanced design techniques such as rounded trench corners or graded oxide thickness to mitigate electric field peaks [35].

These structural differences underscore that leakage current mechanisms are not uniform across SiC MOSFET technologies. Planar designs tend to have lower I_{GSS} under comparable conditions due to simpler oxide fields but pay a penalty in higher on-resistance, while trench designs require careful oxide engineering to balance low on-resistance with acceptable gate leakage performance.

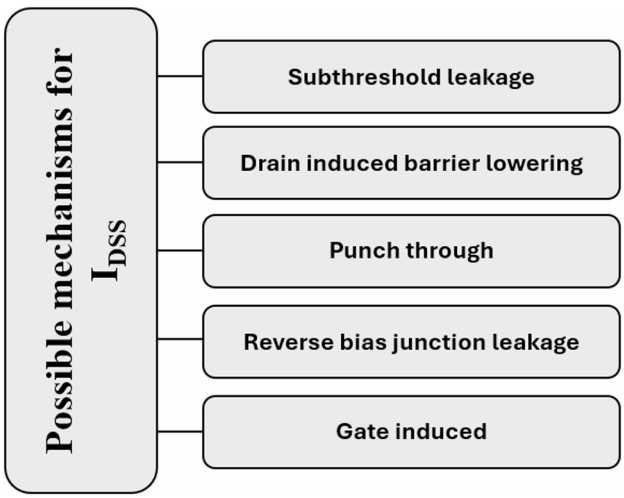


Fig. 5 Mechanisms for I_{DSS}

3 Leakage Current in a Power MOSFET

Leakage current in a MOSFET is the undesirable flow of current between the terminals when the device is ideally meant to remain off. This current can significantly impact power consumption, especially in low-power applications [36].

Drain-to-Source leakage current (I_{DSS}) and Gate-to-Source leakage current (I_{GSS}) are critical parameters for MOSFET characterization and selection [37]. I_{DSS} is the maximum leakage current flowing between the drain and source terminals of a MOSFET when the gate is shorted to the source. It is measured under specific conditions, typically with a defined voltage (V_{DS}) applied between the drain and the source [38]. I_{DSS} is an important parameter for characterizing MOSFET's off-state behavior. A lower I_{DSS} indicates better performance, as it represents less leakage current when the MOSFET is supposed to be off. I_{GSS} is the leakage current flowing between the gate and source terminals of a MOSFET when the drain is shorted to the source [39]. It is measured under specific conditions, typically with a defined voltage (V_{GS}) applied between the gate and the source. I_{GSS} is primarily associated with gate oxide quality. A lower I_{GSS} indicates a better gate oxide, which is crucial for device reliability and performance [40].

3.1 Drain To Source Leakage Current (I_{DSS}) in a MOSFET

In the off-state, a small current still flows from the drain to the source of a MOSFET because the channel is not entirely off [41]. The possible mechanisms responsible for I_{DSS} are summarized in Fig. 5 and are discussed in detail.

3.1.1 Subthreshold Leakage

Subthreshold conduction, also referred to as subthreshold leakage or weak inversion current, is the current that flows between the source and drain of a MOSFET when the transistor operates in the subthreshold region, specifically when the gate-to-source voltage V_{GS} is lower than the threshold voltage V_{th} [42, 43]. This conduction happens because of the emergence of a weak inversion layer [44].

Subthreshold leakage is seen in SiC vertical power MOSFETs, mainly due to trap-assisted conduction, tunneling, and thermionic emission. However, because SiC has a wider bandgap and a lower inherent carrier concentration than Si MOSFETs, the leakage is typically significantly smaller. However, subthreshold performance can be deteriorated by interface traps and high-temperature operation.

Figure 6 shows the energy-band diagram of n-MOSFET, biased such that the surface potential φ_s is less than $2\varphi_B$

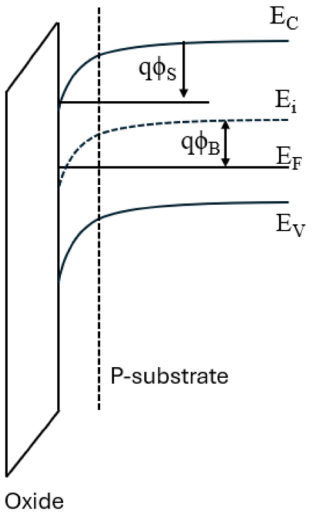


Fig. 6 Band diagram of n-MOSFET in weak inversion mode

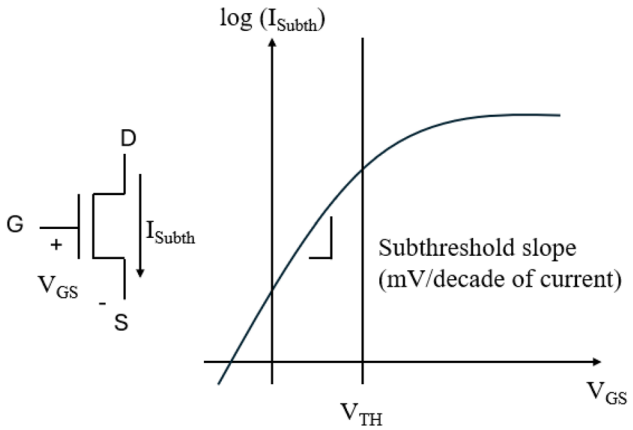


Fig. 7 Subthreshold leakage and slope in an n-MOSFET [46]

(where φ_B is the bulk potential). Because of this biasing, the Fermi level at the gate-substrate interface shifts closer to the conduction band than to the valence band. This causes the semiconductor to behave like a lightly doped n-type material at the interface, allowing a small amount of current to flow. This current is primarily because of the diffusion of minority carriers (electrons in the case of a p-type substrate) in the n-channel [45].

Weak inversion generally predominates the off-state leakage in contemporary devices due to the low threshold voltage. The weak inversion current is described using the following expression (1).

$$I_{ds} = \mu_0 C_{OX} \frac{W}{L}(m-1)(v_T)^2 \times e^{(V_g - V_{th})/mv_T} \times (1 - e^{-v_{DS}/v_T}) \quad (1)$$

where $m = 1 + \frac{C_{dm}}{C_{OX}} = 1 + \frac{\frac{\epsilon_{SiC}}{W_{dm}}}{\frac{\epsilon_{OX}}{t_{OX}}} = 1 + \frac{3t_{OX}}{W_{dm}}$.

In this context, Vth represents the threshold voltage, $V_T = kt/q$ is the thermal voltage, and C_{OX} denotes the gate oxide capacitance. Additionally, μ_0 is the zero-bias mobility, and m is the subthreshold swing coefficient, also known as the body effect coefficient. W_{dm} indicates the maximum depletion layer width, t_{OX} is the gate oxide thickness, and C_{dm} refers to the capacitance of the depletion layer.

For long-channel devices, the subthreshold current remains independent of the drain voltage when V_{DS} exceeds a few v_T.In contrast, the relationship with the gate voltage is exponential, as shown in Fig. 7. The inverse of the slope of $\log_{10}(I_{ds})$ versus VGS is referred to as the subthreshold slope S_t, which can be expressed as follows.

$$S_t = \left[\frac{d(log_{10} I_{ds})}{dV_{gs}}\right]^{-1} = 2.3\frac{mkT}{q} = 2.3\frac{kT}{q}\left(1 + \frac{C_{dm}}{C_{OX}}\right) \quad (2)$$

The sub-threshold slope is an important parameter in analyzing sub-threshold conduction. It reflects how efficiently a transistor can be switched off, representing the rate at which current decreases as the gate voltage is lowered below the threshold voltage.

3.1.2 Drain Induced Barrier Lowering (DIBL)

In long-channel devices, the drain and the source are sufficiently isolated, so their depletion regions do not significantly impact the potential or electric field throughout most of the device. As a result, the threshold voltage in these devices remains largely unaffected by the channel length or drain bias. Nevertheless, in short-channel devices, the depletion regions from the source and drain, along with the source-drain potential, have a substantial influence on band bending across much of the device [47]. Consequently, the threshold voltage and subthreshold current in short-channel devices become dependent on drain bias. This phenomenon is known as drain-induced barrier lowering (DIBL) [48].

In MOSFETs with very short channel lengths, the electric field from the drain can penetrate deep into the channel region [49, 50]. As the drain voltage becomes greater, the electric field from the drain drops the potential barrier at the source end of the channel. This makes it easier for carriers (electrons in n-channel MOSFETs or holes in p-channel MOSFETs) to move from the source to the drain, even if the gate voltage is lower than the threshold. The lowering of the barrier results in a reduction of the threshold voltage, meaning the MOSFET can turn on at lower gate voltages than expected [51].

In comparison to Si MOSFETs, SiC MOSFETs may exhibit a smaller DIBL effect because of the greater electric fields brought about by the material's broad bandgap and

higher breakdown voltage characteristics. It may still affect the off-state characteristics of the device, though, as with any power device, which could result in a rise in leakage currents and possible device performance loss.

3.1.3 Reach Through

Reach-through in a MOSFET is a phenomenon where the source and drain depletion regions combine, allowing current to flow directly from the drain to the source, bypassing the gate control [52, 53]. This occurs at high drain voltages, particularly in short-channel devices, leading to significant leakage currents and potential device failure [54].

In short-channel devices, the closeness of the drain and source results in the depletion regions at the drain-substrate and source-substrate junctions extending into the channel [55]. As the channel length decreases while keeping the doping sustained, the distance between the depletion region boundaries reduces. Raising the reverse bias across the junctions (by raising V_{DS}) brings these junctions even closer. When the channel length and reverse bias combination lead to the depletion regions merging, reach-through occurs [56].

Reach-through can occur in shorter-channel SiC MOSFETs, although it is uncommon. SiC MOSFETs generally operate in the long-channel regime, unlike Si MOSFETs. However, in certain applications, such as low-voltage or high-frequency designs, shorter channel lengths may be used. In these cases, the likelihood of reach-through increases. To mitigate this, the design of the drift region and doping profile is crucial. SiC MOSFETs are carefully engineered with optimized drift regions and doping gradients to minimize reach-through and ensure reliable performance. Proper understanding and mitigation of reach-through are essential for maintaining the reliability and performance of modern MOSFETs, particularly as device dimensions continue to shrink [57].

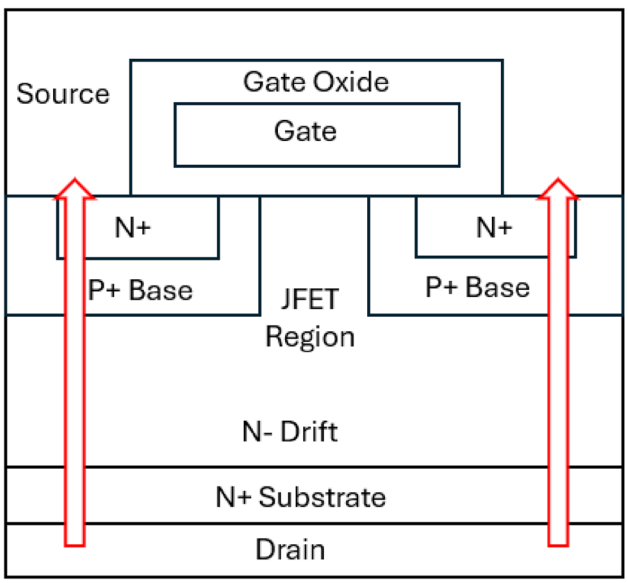


Fig. 8 Reverse-bias pn junction leakage mechanism [61]

3.1.4 Reverse Bias Junction Leakage

The reverse bias junction leakage paths in a SiC power MOSFET are shown in Fig. 8. This leakage can usually occur because of the drift or diffusion of minority carriers in the reverse-bias region, as well as electron-hole pair generation through the avalanche effect [58]. The reverse-bias leakage current in the pn junction is influenced by both the doping concentration and the junction area. In heavily doped pn junctions formed between the drain/source and substrate, the band-to-band tunneling (BTBT) effect predominantly contributes to the reverse bias leakage current [59]. In BTBT, electrons tunnel directly from the valence band of the p-type region to the conduction band of the n-type region [60]. The current density across the reverse-bias pn junction is represented by the following Eq. (3).

$$J_{pn} = A\frac{EV_{app}}{\sqrt{E_g}}exp\left(-B\frac{E_g^{3/2}}{E}\right) \tag{3}$$

Where $A = \frac{\sqrt{2m^*}q^3}{4\pi^3\hbar^2}$ and $B = \frac{4\sqrt{2m^*}}{3q\hbar}$.

In this context, m^* is the effective mass of an electron; E_g is the energy bandgap; V_{app} is the applied reverse bias; E is the electric field across the junction; q is the charge of electrons and $\hbar = h/2\pi$, called reduced Planck's constant. Assuming a step junction, the electric field at the junction can be expressed as shown in Eq. 4.

$$E = \sqrt{\frac{2qN_aN_d(V_{app}+V_{bi})}{\epsilon_{SiC}(N_a+N_d)}} \tag{4}$$

where N_a and N_d are the doping in the p and n side, respectively; ϵ_{SiC} is the permittivity of SiC; V_{bi} is the built-in voltage across the junction. In scaled devices, high doping levels and sharp doping profiles lead to considerable BTBT current across the drain-well junction.

3.1.5 Gate-Induced Drain Leakage (GIDL)

GIDL occurs owing to the high electric field in the overlapping region between the gate and drain. This overlap is inherent in MOSFET fabrication because the gate extends slightly over the drain [62]. During manufacturing, ion implantation for source/drain doping is performed after polysilicon deposition at the gate, causing the dopant atoms to spread laterally into the drain region. Subsequent thermal

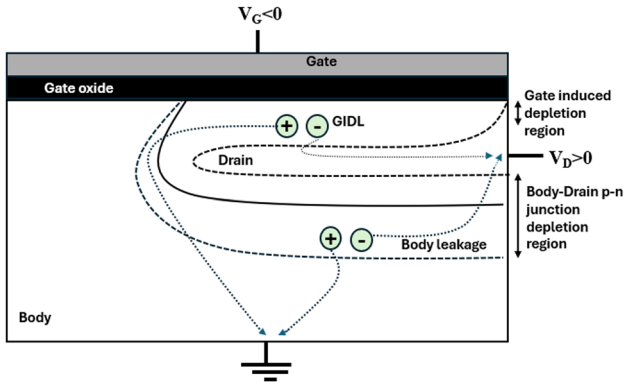


Fig. 9 GIDL in a MOSFET [65]

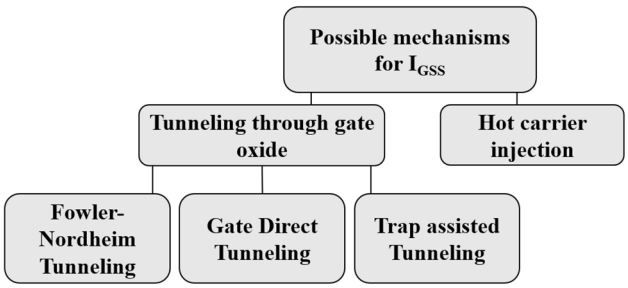


Fig. 10 Mechanisms for I_{GSS}

annealing, which reduces defects, also raises the lateral diffusion of these dopants. When a voltage is applied to the drain while $V_{GS} < 0$, significant band bending occurs in the overlapped drain region, triggering band-to-band tunneling of electrons. This tunneling produces electron-hole pairs that may be swept into the drain and substrate, as depicted in Fig. 9. This process is known as Gate-Induced Drain Leakage (GIDL) [63].

One crucial area of a SiC power MOSFET's design is the gate-drain overlap zone, where the gate voltage can affect the electric field distribution. Electron-hole pairs can be formed in the depletion area if the gate voltage is high enough to provide a strong electric field, particularly under reverse bias conditions. These carriers may add to the leakage current if they are swept in the direction of the drain. Although this effect is comparable to that seen in Si-based MOSFETs, the actual behavior of this phenomenon varies slightly because of SiC's wide bandgap.

GIDL results from electrons tunneling from the filled valence band in the drain near the surface to the unoccupied conduction band further away. Proper drain design can help mitigate GIDL [64] using a lightly doped drain near the channel can lower this leakage by increasing the depletion region width.

3.2 Gate To Source Leakage Current in a MOSFET (I_{GSS})

I_{GSS} is primarily due to tunneling currents through the gate oxide or gate leakage currents. It is the current that leaks from the gate terminal to the source terminal when the gate-source voltage is applied [66]. This current is a crucial indicator of SiC MOSFET degradation [67]. The possible mechanisms responsible for I_{GSS} are summarized in Fig. 10 and are discussed in detail.

3.2.1 Tunneling Through Gate Oxide

The tunneling mechanism between the substrate and the gate polysilicon is categorized into two main types: (1) Fowler–Nordheim (FN) tunneling and (2) direct tunneling. In addition to these two mechanisms, trap-assisted tunneling through localized trap states can also cause significant leakage [18]. The probability of tunneling for an electron is influenced by factors such as the barrier thickness, barrier height, and the specific barrier structure. As a result, the probability of tunneling for a single electron differs between FN tunneling and direct tunneling, leading to variations in the tunneling currents [68].

Direct tunneling and Fowler-Nordheim (FN) tunneling are of lesser significance in SiC power MOSFETs than in ultra-thin oxide devices, including planar CMOS transistors. Since the possibility of tunneling diminishes exponentially with increasing oxide thickness, the thicker gate oxides in SiC MOSFETs—typically in the 50–100 nm range—significantly lower the probability of direct tunneling. However, at extremely high electric fields, such as during overvoltage situations where the rated gate voltage is exceeded, FN tunneling may take place. It is a non-dominant process, though, because these electric fields are usually well below the threshold needed for FN tunneling under typical operating conditions.

3.2.1.1 ***Fowler-Nordheim Tunneling*** In Fowler–Nordheim (FN) tunneling, electrons move from the conduction band of the semiconductor into the conduction band of the oxide layer [69]. Figure 11 illustrates the FN tunneling process, where electrons move from the inverted surface to the gate. When disregarding the impacts of temperature and image-force-induced barrier lowering, the current density associated with FN tunneling can be given by Eq. 5.

$$J_{FN} = \frac{q^3 E_{OX}^2}{16\pi^2 \hbar \varphi_{OX}} \exp\left(-\frac{4\sqrt{2m^*}\,\varphi_{OX}^{3/2}}{3\hbar q E_{OX}}\right) \tag{5}$$

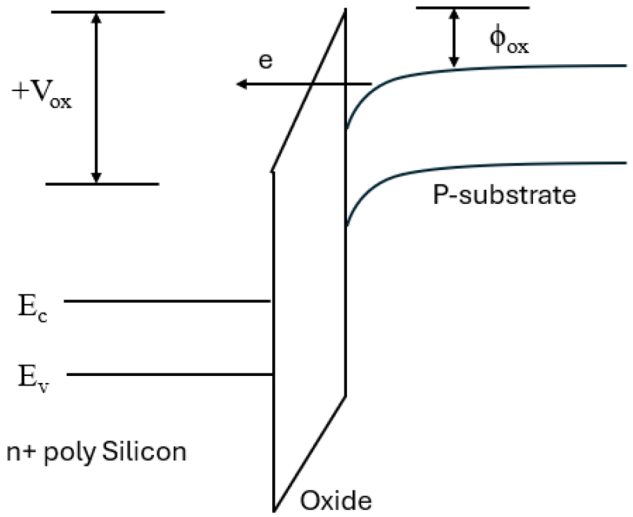


Fig. 11 FN tunneling mechanism [70]

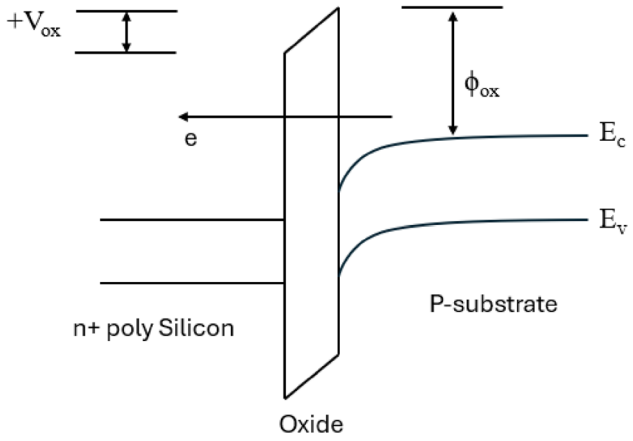


Fig. 12 Direct tunneling mechanism [70]

In this context, E_{OX} denotes the electric field across the oxide, φ_{OX} represents the barrier height for electrons within the conduction band, and m^* refers to the effective mass of an electron in the Si conduction band. The Fowler–Nordheim current equation describes the tunneling process through a triangular potential barrier and is applicable when $V_{OX} > \varphi_{OX}$, where V_{OX} is the voltage drop across the oxide layer. The measured FN tunneling current is generally quite low.

3.2.1.2 Gate Direct Tunneling Direct tunneling current is prominent when the thickness of the oxide is minimal. In extremely thin oxide layers (typically less than 3–4 nm), electrons from the inverted Si surface tunnel directly to the gate via the forbidden energy gap of the SiO layer, rather than entering the conduction band of SiO [71]. Figure 12 illustrates this direct tunneling phenomenon. In this scenario, electrons pass through a trapezoidal potential barrier, not a triangular one. Consequently, direct tunneling takes

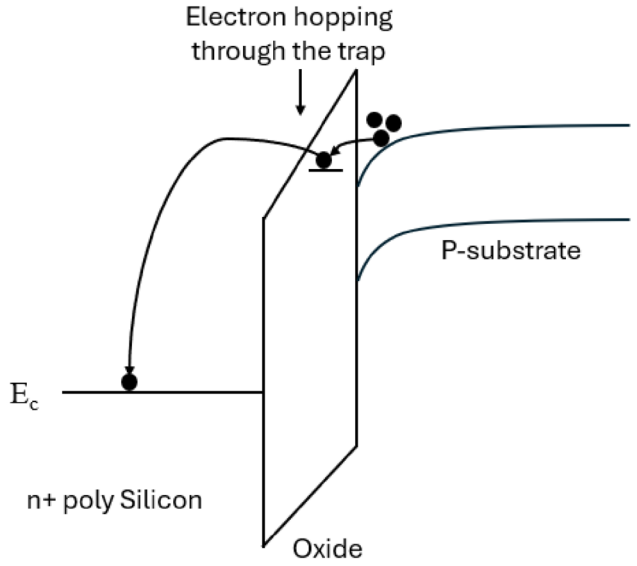


Fig. 13 Trap-assisted tunneling mechanism [70]

place when $V_{OX} < \varphi_{OX}$. The equation that describes the current density for direct tunneling is as follows:

$$J_{DT} = AE_{OX}^2 \exp\left\{-\frac{B(1-\left[1-\frac{V_{OX}}{\varphi_{OX}}\right]^{3/2}}{E_{OX}}\right\} \quad (6)$$

where $A = q^3/16\pi^2\hbar\varphi_{OX}$

$B = 4\sqrt{2m^*}\,\varphi_{OX}^{3/2}/3\hbar q$

.

Since the gate oxides of SiC MOSFETs are far thicker (usually 50–100 nm) than the ultra-thin oxides (less than 3–4 nm) seen in planar CMOS devices, direct tunneling is practically insignificant in these devices under typical operating conditions. The likelihood of electrons tunneling directly through the forbidden energy gap rapidly drops with increasing oxide layer thickness, as direct tunneling is an exponential function of oxide thickness. Therefore, even though the direct tunneling process is theoretically possible, the thick oxide architecture of SiC MOSFETs prevents it from significantly causing gate leakage.

3.2.1.3 Trap-assisted Tunneling Trap-assisted tunneling is a process where electrons move through the gate oxide by hopping through localized trap states, which arise from defects or impurities in the oxide layer or at the SiC/SiO_2 interface, as illustrated in Fig. 13 [72]. These trap states, located deep within the energy gap of the oxide layer, act as charge centers, facilitating electron transitions from the

inversion layer to the trap sites. The likelihood of electron capture depends on the distribution of these traps in both energy space and physical location. In SiC MOSFETs, such defects are often attributed to intrinsic imperfections during oxide growth or to stress-induced defects at the SiC/SiO_2 interface.

Electron transport through these traps involves multiple hopping transitions, typically assisted by phonons, with the hopping conduction being limited by the spatial distribution of traps. This behavior can significantly influence the gate leakage current in SiC power MOSFETs. To model trap-assisted leakage currents, many approaches assume a simplified continuous capture cross-section for all trap states. However, the actual traps are distributed non-uniformly, both in energy and spatially, and their capture cross-sections vary depending on their depth within the oxide and their energy levels [73].

In the context of SiC MOSFETs, the traps include (i) fixed charges formed during fabrication, (ii) mobile charges that can migrate under electric fields, (iii) interfacial trapped charges at the SiC/SiO_2 interface with energy levels spread across the forbidden energy gap, and (iv) oxide-trapped charges within the bulk of the oxide, often arising from oxygen vacancies or other intrinsic defects. These charge centers can degrade device performance by contributing to gate leakage currents and affecting reliability [74]. Understanding the distribution and behavior of these traps is crucial for improving the performance and reliability of SiC power MOSFETs, particularly under high electric field conditions.

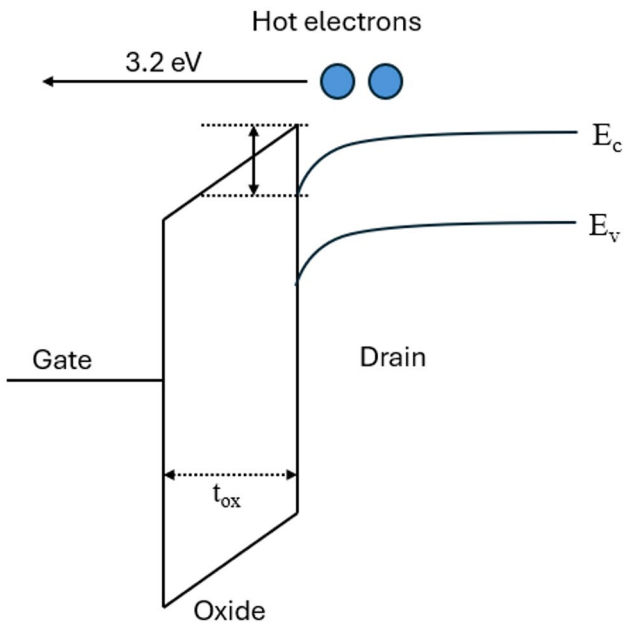


Fig. 14 Hot electron injection [70]

3.2.2 Hot Carrier Injection

Hot Carrier Injection (HCI) is a significant degradation mechanism in MOSFETs, especially in high electric field conditions where carriers gain sufficient kinetic energy to become 'hot' and are injected into the gate oxide layer [75]. When the device operates under high drain-to-source voltages, electrons or holes in the channel can acquire high energy and penetrate the gate oxide. This phenomenon introduces trap sites and defects within the oxide, altering its structural integrity and leading to an increase in gate-to-source leakage current (I_{GSS}).

In SiC MOSFETs, which are designed for high-voltage applications, the effects of HCI are particularly pronounced [76]. HCI-induced traps create regions within the oxide that facilitate carrier tunneling from the gate to the source. This carrier tunneling is further exacerbated by Stress-Induced Leakage Current (SILC), another key reliability issue in MOSFETs [77]. SILC arises due to prolonged electrical stress across the gate oxide, which contributes to additional trap sites and increases leakage paths. As HCI generates initial trap sites, the sustained high electric fields intensify SILC by enabling carriers to tunnel more easily through the thinner, degraded oxide regions. Consequently, the combination of HCI and SILC amplifies I_{GSS}, causing a substantial rise in leakage current over time. This dual effect not only compromises gate control over the channel but also accelerates the degradation of threshold voltage stability and overall device longevity [78, 79]. Figure 14 illustrates the energy band diagram in terms of hot electron injection.

4 Factors Affecting the Leakage Current of a MOSFET

Leakage currents in MOSFETs, specifically I_{DSS} (Drain-Source leakage current with Gate shorted) and I_{GSS} (Gate-Source leakage current with Drain shorted), are influenced by a myriad of intrinsic and extrinsic factors [80]. The channel dimensions, particularly the length and width, significantly impact I_{DSS}, as shorter channels heighten electric fields and enhance tunneling currents [81]. Doping concentration plays a crucial role, where higher doping can mitigate subthreshold conduction yet potentially increase junction leakage [82]. The quality and thickness of the gate oxide are paramount, with thinner oxides and defects promoting gate-induced drain leakage (GIDL) [83]. Elevated temperatures universally augment leakage currents by boosting carrier generation rates. Surface states and interface traps, especially at the SiC/SiO_2 interface, contribute to trap-assisted tunneling, exacerbating leakage [84]. High electric fields further elevate leakage through mechanisms

such as band-to-band tunneling, while higher drain-source voltages (V_{DS}) amplify the electric field within the device, leading to increased leakage [85]. Y. Xiao et al. studied the long-term reliability of SiC MOSFETs under total ionizing dose (TID) effects, revealing that gate leakage current degradation depends on the bias voltage. At a critical gate bias, the leakage current increases then decreases, and finally grows exponentially before oxide breakdown. This behavior is driven by sequential hole trapping, interface trap de-passivation, and electron trapping during Fowler–Nordheim (FN) tunneling, with FN tunneling identified as the primary conduction mechanism [86]. Besides, manufacturing defects can be another factor that provides unintended paths for leakage currents.

The gate material's work function relative to the semiconductor affects the barrier height and consequently the leakage [87]. High electric fields across the gate oxide, influenced by bias conditions, can induce significant tunneling currents. Similarly, higher temperatures elevate I_{GSS} as well by enhancing carrier generation and reducing tunneling barriers. Interface traps and defects at the gate oxide/semiconductor interface facilitate trap-assisted tunneling, further increasing leakage [69].

In SiC MOSFETs, the higher density of defects compared to Si can lead to increased leakage through defect states [88]. Oxide reliability issues, including higher interface state densities and oxide charge trapping, are more pronounced in SiC MOSFETs [89]. Despite the superior thermal conductivity of SiC, localized heating at defect sites can still exacerbate leakage currents. Surface roughness prior to oxide deposition impacts oxide quality and subsequent leakage [90]. Understanding these factors is crucial for optimizing the design and performance of MOSFETs to minimize leakage currents and enhance device reliability. The impact of packaging materials on leakage currents was investigated by M. A. Alam et al. [91]. Their findings suggest that the properties of molding compounds can influence the magnitude of leakage currents, emphasizing the importance of material selection in MOSFET manufacturing.

Building upon the understanding of degradation mechanisms, J. P. Kozak et al. introduced a robustness testing methodology for SiC MOSFETs [92]. Their work reinforced the dominance of gate oxide degradation as a failure mode under high-stress conditions. While gate oxide and bulk semiconductor degradation are critical concerns, the inherent structure of MOSFETs contributes to leakage currents as well. D. Mukherjee and B. V. R. Reddy [93] focused on reducing p-n junction leakage by modifying MOSFET construction. Their simulations demonstrated that terminating the junctions with silicon dioxide can significantly decrease substrate leakage.

The effect of MOSFET architecture can also be profound on the leakage current. The study by S. Yadav et al. employed three-dimensional modeling to investigate gate leakage characteristics within various nanoscale MOSFET architectures, encompassing fin field-effect transistors and gate-all-around MOSFETs. Direct quantum tunneling-based gate leakage currents were computed using the Wentzel-Kramers-Brillouin approximation. Quantum transport calculations for gate leakage current were conducted through the non-equilibrium Green's function formalism. Among the investigated MOSFET structures, the gate-all-around MOSFET exhibited the most pronounced correlation between gate leakage and variations in gate material work function and oxide thickness [94].

The study by Y. Zhou et al. develops a model to understand how SiC MOSFETs fail during short circuits. The model focuses on leakage currents and the build-up of electric charge at the interface between the SiC and its insulating layer. The main leakage current flows through a specific part of the device and is influenced by several factors. The amount of electric charge at the interface affects how well the device conducts electricity. The researchers believe that two types of current, which increase as the device gets hotter, are primarily responsible for the failure of the device. As the leakage current grows, it causes the device to heat up even more, creating a harmful cycle that leads to failure [95].

A similar study by H. Nemoto et al. examined the contribution of electrons and holes to the leakage current in p-channel 4 H-SiC MOSFETs when a negative voltage is applied to the gate. It was found that electrons primarily cause leakage when the gate is made of n+polysilicon. The leakage behavior of electrons follows two specific mechanisms: Fowler-Nordheim and Pool-Frenkel. However, assessing the hole leakage current was hindered by the injection of hot electrons from the gate electrode side [96]. A similar study carried out by W. Tan et al. investigates how and why current flow changes in 1.2 kV SiC MOSFETs under different operating conditions. By combining computer simulations, experiments, and data analysis, the authors identified the mechanisms responsible for increased current leakage. It was found that trap-assisted tunneling and Fowler-Nordheim tunneling cause leakage when the device is under normal operating conditions. However, under extreme conditions, the build-up of trapped particles within the device accelerates its breakdown. In addition, the authors observed that electrons can also cause leakage, leading to the creation of defects at the interface between the SiC and its insulating layer [97]. Figure 15 presents a summary of factors affecting leakage current in MOSFET.

To enhance the depth and clarity of the analysis, Table 1 presents a consolidated summary of key findings from the

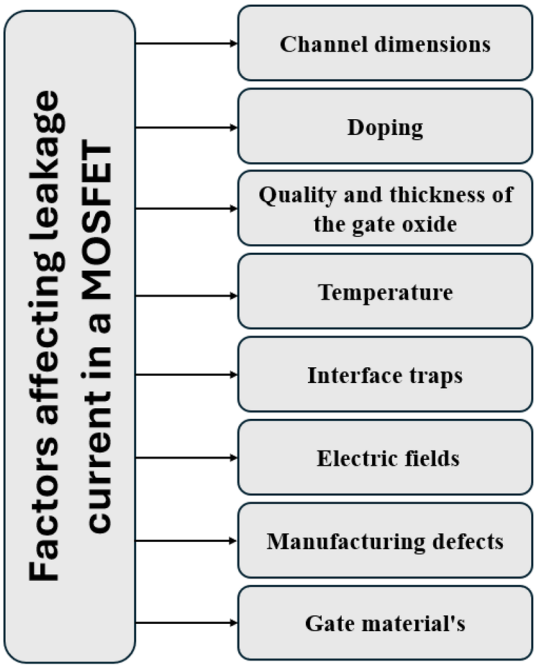


Fig. 15 Factors affecting leakage current in a MOSFET

previously discussed studies on leakage current mechanisms in SiC MOSFETs. This table encapsulates the critical experimental conditions, modeling approaches, dominant conduction mechanisms, and the corresponding insights into device behavior under various electrical, thermal, and structural stressors. By organizing the literature in this comparative format, the table enables a clearer understanding of how factors such as gate bias, device architecture, interface quality, temperature, and packaging materials contribute to leakage current phenomena. Notably, it underscores the recurring significance of Fowler-Nordheim tunneling, trap-assisted tunneling, and defect-mediated conduction as the primary leakage pathways reported across diverse operational regimes.

To provide a clearer visualization of how different stress conditions influence leakage current mechanisms in SiC MOSFETs, a conceptual summary is presented in Fig. 16. This figure qualitatively maps the relative contribution of four key leakage pathways: Fowler-Nordheim tunneling, trap-assisted tunneling, thermally activated leakage, and interface charge effects under various stress environments, including high gate bias, elevated temperature, ionizing radiation, and packaging-induced stress. The severity levels are based on findings consolidated from the studies presented in Table 1 above, offering an intuitive comparison across operating conditions. This visual representation complements the tabulated data and emphasizes the multifactorial nature of leakage behavior, reinforcing the need for holistic reliability assessment strategies in SiC MOSFET design and application.

Table 1 Summary of reported studies on leakage current mechanisms in SiC mosfets

Reference	Stress condition	Dominant mechanism	Findings
Y. Xiao et al. [86]	Total ionizing dose (TID), varying gate bias	FN tunneling, hole/electron trapping	Gate leakage increases, then drops before an exponential rise, as oxide breakdown under critical bias.
M. A. Alam et al. [91]	Packaging effects	Thermally activated leakage paths	Molding compound properties influence leakage, highlighting the packaging material.
J. P. Kozak et al. [92]	High-stress reliability testing	Gate oxide degradation	Robustness testing reinforces oxide degradation as the main failure mode.
D. Mukherjee and B. V. R. Reddy [93]	Device structure modification	pn junction leakage	SiO_2-terminated junctions reduce substrate leakage currents in simulations.
S. Yadav et al. [94]	Nanoscale architectures (GAA, FinFET)	Direct tunneling, quantum transport	Gate-all-around MOSFET shows the highest leakage sensitivity to work function and oxide thickness.
Y. Zhou et al. [95]	Short-circuit failure modeling	Interface charge accumulation	Leakage-driven self-heating feedback loop leads to failure.
H. Nemoto et al. [96]	p-channel 4 H-SiC MOSFETs, negative bias	Fowler–Nordheim, Pool-Frenkel	Electron-dominated leakage; hole leakage assessment limited by hot electron injection.
W. Tan et al. [97]	High-voltage (1.2 kV) MOSFET operation	Trap-assisted tunneling, FN tunneling	Leakage increases under stress; trapped charge buildup accelerates breakdown.

5 Radiation-Induced Leakage Current and its Impact on SiC MOSFET Working

Leakage current in MOSFETs critically affects their performance and, consequently, the overall system efficiency and reliability [98]. Elevated leakage currents lead to increased power consumption, which is particularly detrimental in

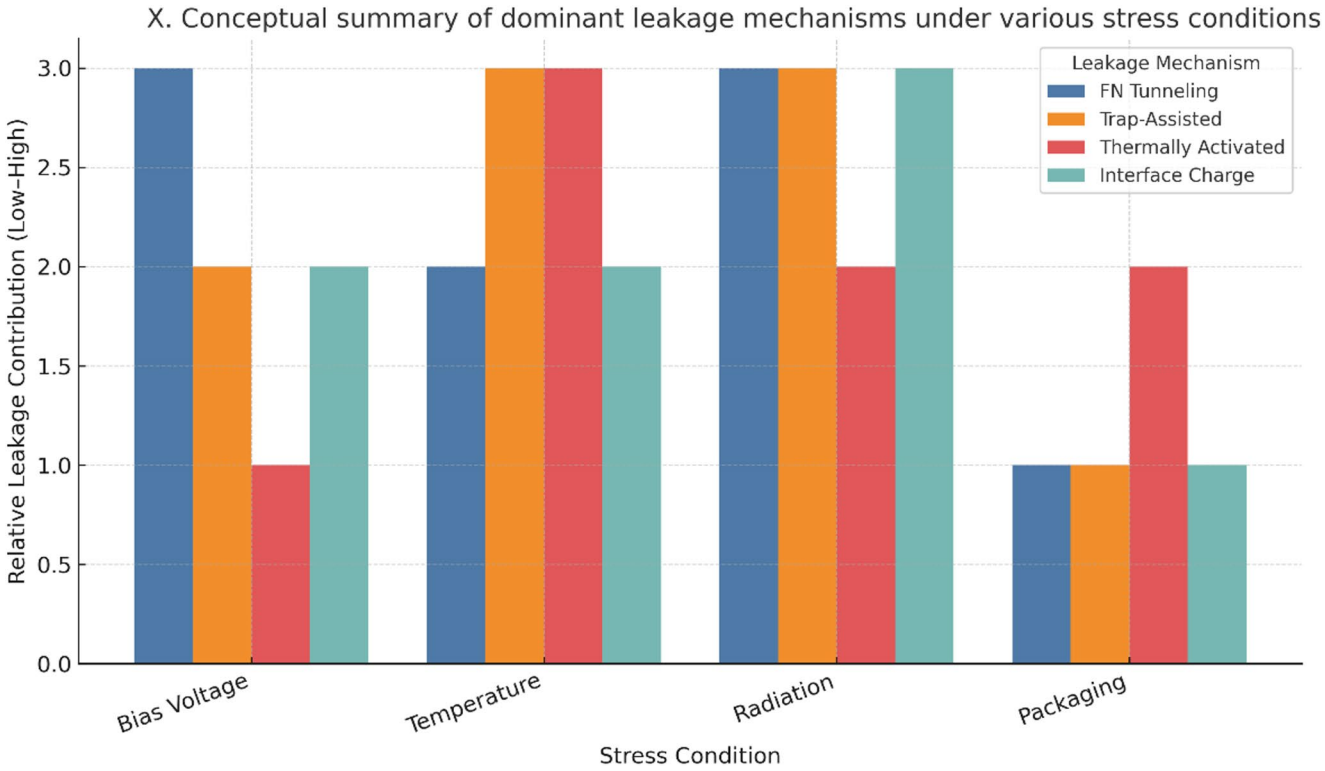


Fig. 16 Conceptual summary of dominant leakage mechanisms under various stress conditions

low-power applications, reducing battery life and overall energy efficiency [99]. Furthermore, excessive leakage can cause thermal runaway, where the heat generated from leakage exacerbates the current, potentially leading to device failure [100]. In digital circuits, leakage currents can cause logic errors, affecting data integrity and leading to malfunction [101]. In analog circuits, leakage currents can introduce noise and offset errors, degrading signal fidelity and accuracy [102]. Additionally, an increase in gate-to-source leakage current (I_{GSS}) can stress the gate oxide layer, accelerating oxide degradation. If I_{GSS} continues to rise, the intense electric field across the gate oxide can lead to oxide breakdown, resulting in permanent damage and potential short-circuiting of the device. Xi et al. [103] examined the long-term degradation of SiC MOSFETs in a power factor correction converter. They observed a significant increase in both drain-source and gate leakage currents due to gate oxide degradation. J. P. Kozak et al. [19] further explored the degradation mechanisms of SiC MOSFETs under harsh switching conditions, identifying two primary causes: gate oxide degradation and bulk semiconductor degradation. These studies highlight the detrimental effects of high electric fields and temperatures on MOSFET reliability.

Radiation-induced leakage current (RILC) in SiC MOSFETs poses significant challenges to their performance and reliability in radiation-prone environments such as space and aerospace systems. The unique material properties of SiC provide inherent radiation hardness; however, exposure to ionizing radiation and heavy-ion irradiation can significantly impact device performance, particularly through mechanisms that induce leakage currents and degrade the gate oxide.

One primary mechanism contributing to RILC in SiC MOSFETs is trap-assisted tunneling (TAT). In thermally grown oxides on 4 H-SiC, defects such as carbon-related defects or oxygen vacancies generate energy states in the oxide bandgap. These states facilitate charge trapping and tunneling through the oxide, leading to increased leakage currents, particularly at higher radiation doses. Heavy-ion irradiation also induces transient conductive paths, further contributing to leakage current [72]. Another notable mechanism involves the formation of leakage paths due to parasitic bias effects caused by the accumulation of positive charges in the field oxide. This phenomenon is independent of SiC/oxide interface degradation and predominantly influences leakage currents as radiation doses increase [104].

Heavy-ion irradiation has been observed to cause permanent degradation in SiC MOSFETs, leading to increased drain and gate leakage currents. The leakage paths manifest differently depending on the bias conditions: under low drain bias, leakage occurs between the drain and gate, while higher bias conditions result in leakage from the drain to the source [105]. Moreover, the increase in leakage currents correlates with the heavy-ion fluence, highlighting the

gradual degradation of the gate oxide and the blocking capabilities of the device [106].

Total ionizing dose (TID) radiation also impacts SiC MOSFETs by introducing trapped charges at the SiO_2/SiC interface. This trapped charge forms an inversion layer during the off-state, resulting in increased leakage currents and threshold voltage shifts [107]. Additionally, TID effects exacerbate atomic displacement and defect generation in the gate oxide, further contributing to leakage through TAT mechanisms [108].

Defects induced by radiation, particularly in the gate oxide, significantly threaten the long-term reliability of SiC MOSFETs. Atomic displacement defects and electrical stress defects create leakage paths in the devices under heavy irradiation, even when displacement damage (DD) results show no immediate effects on the electrical characteristics of the device under test (DUT). These leakage paths degrade device reliability, reduce operational lifetime, and necessitate robust design strategies to mitigate radiation-induced degradation [109].

Despite these challenges, SiC MOSFETs exhibit remarkable radiation hardness compared to their Si counterparts. Studies have shown negligible changes in subthreshold drain current and breakdown voltage in SiC devices exposed to irradiation, suggesting improved gate oxide quality and reduced susceptibility to typical Si MOSFET failure mechanisms such as hole and electron tunneling [110]. However, catastrophic damage, such as single-event burnout (SEB) under specific conditions, remains a concern [111]. Understanding and mitigating RILC is critical for ensuring the reliable operation of SiC MOSFETs in radiation-prone applications.

In space environments, where radiation exposure is inevitable, understanding and mitigating RILC in SiC MOSFETs is critical for ensuring reliable operation. Test methodologies must account for the impact of increased leakage currents on single-event effect susceptibility and overall device performance [112]. SiC MOSFETs remain a promising candidate for space applications, provided these radiation-induced challenges are addressed through advanced material engineering and circuit design strategies. Table 2 provides a summary and some quantitative analysis of Gate and Drain Leakage Current Behavior in SiC MOSFETs discussed above.

Table 2 Summary of gate and drain leakage current behavior in SiC mosfets under various stress conditions

Reference	Stress condition	I_{GSS}	I_{DSS}	Remarks
Xi et al. [103]	Long-term aging in the PFC converter at 1200 V	+2.9 nA (MOS-A), +5 pA (MOS-B)	1.3 nA → 3.98 µA (MOS-A), 0.6 nA → 276 µA (MOS-B)	Significant leakage increase, but no breakdown voltage degradation
J. P. Kozak et al. [19]	Hard switching at 25 °C and 100 °C	Failure at mA-level: 30 min (100 °C), 50 h (25 °C)	~10× increase at 600 V; >100× at 1200 V	Accelerated failure at high temperature and switching bias
C. Martinella et al. [105]	Heavy-ion irradiation (56Fe, 82Kr, 131Xe)	Gate leakage increases per ion fluence; steps observed	Drain leakage increases per ion fluence; steps observed	Drain–gate leakage at ≤350 V; drain–source at higher bias
C. Martinella et al. [106]	Heavy-ion Au irradiation	Steps > 2.5 nA per ion; cumulative increase of hundreds of nA	Cumulative degradation in the hundreds nA range	Leakage is consistent but with local variations due to fabrication and measurement
M. Alexandru et al. [110]	Charged particle irradiation	Negligible change	Negligible change	Demonstrates superior SiC radiation hardness vs. Si

To further support the understanding of radiation-induced leakage currents in SiC MOSFETs, an experimental study was performed to examine the effects of neutron irradiation on leakage characteristics. The device under test (DUT) was a Toshiba TW048N65C SiC MOSFET in TO-247 packaging with a peak reverse voltage rating of 650 V. Neutron irradiation was carried out using the TRIGA Mark II research reactor at the Nuclear Power Division, Agency Nuclear Malaysia (ANM). The fluences of 4×10^{14} cm^{-2} and 5×10^{14} cm^{-2} were chosen for this study. Leakage characterization was performed before and after irradiation using a Keithley 4200 SCS parameter analyzer. The I_{GSS} was measured as a function of V_{GS}, while the I_{DSS} was measured as a function of V_{DS}.

The experimental results show a clear increase in both I_{GSS} and I_{DSS} following neutron irradiation. While I_{GSS} exhibited a modest increase, I_{DSS} demonstrated a more pronounced rise with higher neutron fluence. This behavior is consistent with radiation-induced defect generation in the gate oxide and semiconductor bulk, which can facilitate tunneling and increase leakage pathways. Figures 17 and 18 illustrate the measured I_{DSS}–V_{GS} and I_{GSS}–V_{DS} characteristics, respectively, showing the systematic shift toward higher leakage levels post-irradiation.

These findings reinforce the concerns highlighted in the literature about the vulnerability of SiC MOSFETs to radiation-induced leakage currents, even though they exhibit excellent overall radiation hardness. They underscore the need for continued development of radiation-hardened design strategies and careful qualification of SiC power devices for deployment in neutron-rich or space

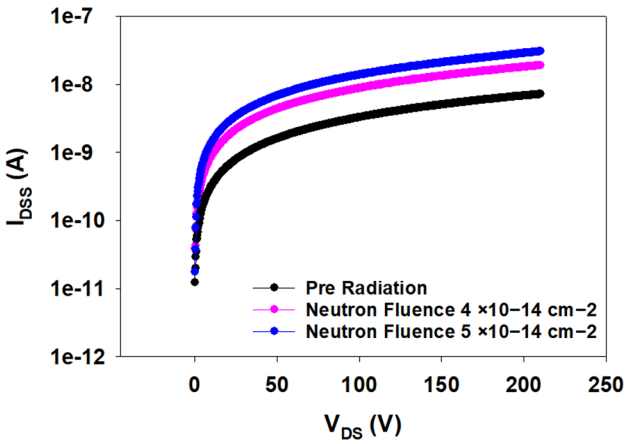


Fig. 17 I_{DSS} characteristics of Toshiba TW048N65C SiC MOSFET post-neutron irradiation

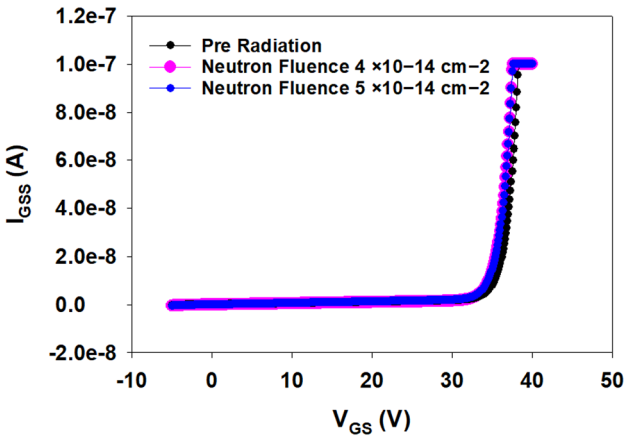


Fig. 18 I_{GSS} characteristics of Toshiba TW048N65C SiC MOSFET post-neutron irradiation

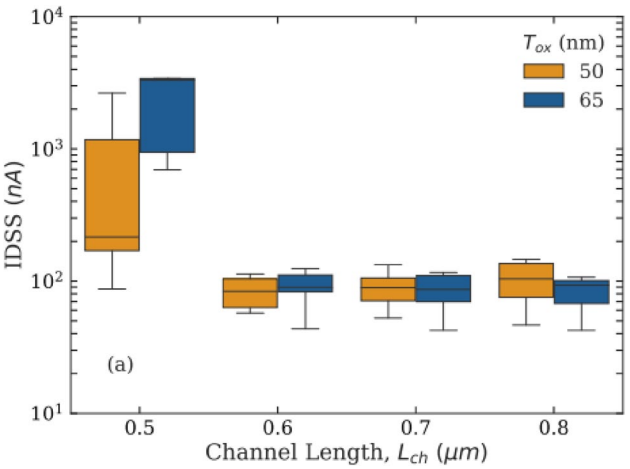


Fig. 19 Drain to source leakage current dependence on channel length in a 3.3 kV SiC MOSFET

environments. By presenting these results, this work aims to provide additional empirical evidence supporting ongoing efforts to understand and mitigate radiation-induced degradation in SiC MOSFETs.

6 Mitigation Strategies

To reduce I_{DSS} and I_{GSS} in SiC MOSFETs, several techniques can be applied, focusing on both material properties and device engineering [113]. This section presents an overview of the mitigation strategies for reducing leakage in MOSFET.

Optimizing the doping profile and channel length can minimize I_{DSS} by reducing off-state leakage [114]. Research conducted by S. Rathi et al. on 3.3 kV VDMOSFET demonstrates that reducing the channel length to 0.5 µm leads to a substantial increase in I_{DSS}, as evident in Fig. 19 [115]. The figure shows that I_{DSS} exceeds 1000 nA at 0.5 µm, while for channel lengths $\geq$ 0.6 µm, I_{DSS} drops below 200 nA. This behavior reflects short-channel effects that weaken gate control and increase off-state leakage. The comparison between oxide thicknesses (50 nm vs. 65 nm) also suggests that thicker oxides may exacerbate leakage at very short channel lengths.

Apart from this, incorporating field plates can help in modulating the electric field distribution within the device, thus reducing both I_{DSS} and I_{GSS} [116]. Using techniques like retrograde well doping and pocket implants can help control short-channel effects, which contribute to leakage currents [117]. In addition to this, using high-purity, low-defect semiconductor materials can significantly reduce leakage currents by minimizing recombination centers and traps that contribute to leakage [118]. SiC wafers inherently have a higher defect density compared to Si. Advanced manufacturing processes like epitaxial growth and substrate polishing can reduce defect densities, leading to lower leakage currents [119].

Adjusting the doping profile in MOSFETs also helps to reduce leakage currents by optimizing the electric field distribution, which lowers hot carrier injection and minimizes band-to-band tunneling [65]. A gradual doping gradient in the drain and channel regions reduces peak electric fields, preventing gate-induced leakage, while controlled substrate doping maintains a higher threshold voltage, reducing off-state leakage. These adjustments collectively enhance device reliability and lower power losses without compromising performance [120]. Apart from this, choosing a metal gate material with an appropriate work function can help control the threshold voltage and reduce gate leakage [121]. In some advanced designs, dual-gate structures can be utilized to provide superior control over the channel, thereby

reducing leakage. Optimizing post-fabrication annealing processes, such as rapid thermal annealing (RTA), can help reduce defects and trap densities, leading to lower leakage currents [122].

The leakage current through thin gate oxides can be mitigated by utilizing high-k dielectric materials, like HfO_2, Al_2O_3, and Ta_2O_5 [123]. Substituting the SiO_2 layer with a thicker layer of high-k dielectric achieves a capacitance comparable to that caused by a thinner layer of low-k dielectric (SiO_2) [124]. This substitution effectively reduces leakage caused by tunneling. However, selecting appropriate high-k material poses challenges, as it must establish a superior interface with Si, possess higher resistivity, and maintain thermal stability. Figure 20(a) illustrates the device structure with a low-k dielectric, while Fig. 20(b) depicts the structure incorporating a high-k dielectric in conjunction with a low-k dielectric, resulting in a decrease in leakage current [65].

Another important factor to consider regarding MOSFET leakage currents is the use of high-quality gate oxides with minimal interface traps and low charge densities. The use of advanced oxidation techniques, like thermal oxidation followed by post-oxidation annealing, can improve the oxide quality [125]. Increasing the thickness of the gate oxide can reduce I_{GSS} by providing a stronger barrier to electron tunneling [126]. However, this must be balanced with the need for sufficient gate capacitance. Implementing passivation layers (e.g., SiO_2 or Si_3N_4) can reduce the interface states that contribute to gate leakage.

7 Future Trends and Research Directions

As SiC MOSFET technology continues to evolve, several emerging trends and potential advancements are expected to shape the future landscape of power electronics [127]. These developments focus on improving device performance, particularly in reducing leakage currents, which remain a critical challenge for enhancing the efficiency and reliability of SiC-based systems.

One of the most promising trends in SiC MOSFET technology is the continued refinement of material quality and processing techniques [128]. Advances in epitaxial growth, doping control, and defect reduction are expected to yield SiC MOSFETs with lower intrinsic defect densities, thereby reducing leakage currents and enhancing device performance. The integration of innovative device architectures, such as trench MOSFETs and super junction structures, is also gaining traction [129]. These architectures offer potential improvements in channel mobility and breakdown voltage, which could further mitigate leakage issues while enabling higher power densities. Recent studies comparing asymmetric trench and double-trench SiC MOSFETs under repetitive avalanche stress reveal distinct degradation patterns between these designs. The double-trench MOSFET improves conduction characteristics but experiences a significant increase in gate-drain capacitance due to positive charge injection at the bottom gate oxide. In contrast, the asymmetric trench MOSFET shows stable capacitance yet suffers from a more pronounced decrease in threshold voltage, with higher stress in its inclined channel. These findings underscore the importance of optimizing trench architectures to balance performance and reliability in future SiC MOSFET advancements [130]. Figure 21shows the cross-section of double-trench and asymmetric-trench SiC MOSFETs.

Additionally, the development of hybrid SiC devices, which combine SiC MOSFETs with other wide-bandgap materials like GaN, is an emerging trend that could lead to new performance benchmarks [131]. These hybrid devices could leverage the complementary strengths of different materials to achieve lower leakage currents, higher switching speeds, and improved thermal management. Figure 22 shows a GaN-based HEMT (high-electron mobility transistor) with a SiC-type substrate. GaN-based power devices, particularly HEMTs, are advancing due to their ability to support high current, voltage, and low ON-state

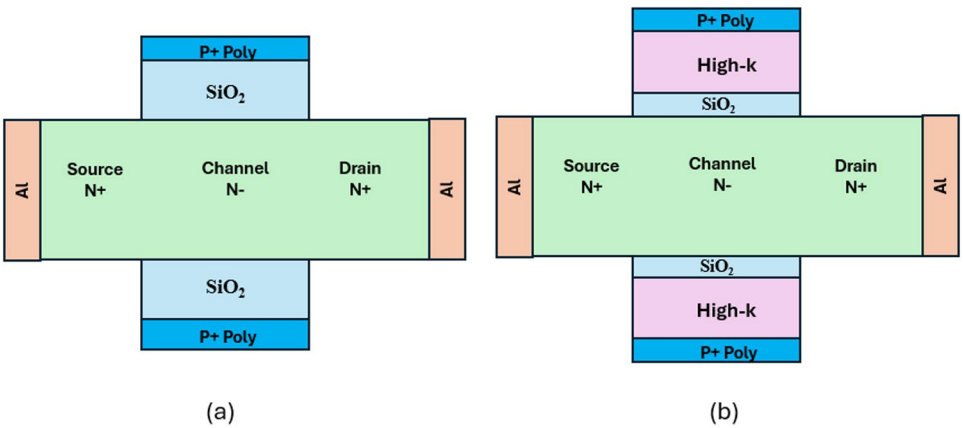


Fig. 20 A device (**a**) without high k dielectric and (**b**) with high k dielectric

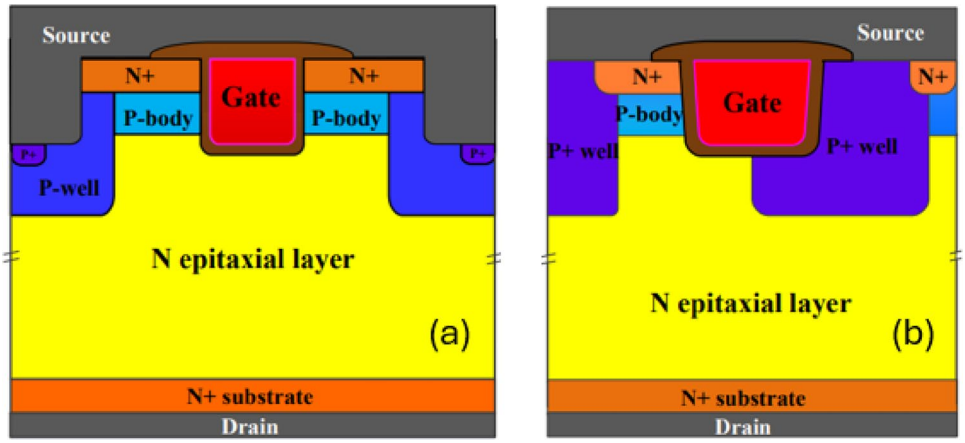


Fig. 21 Schematic of double trench and asymmetric trench SiC MOSFETs [130]

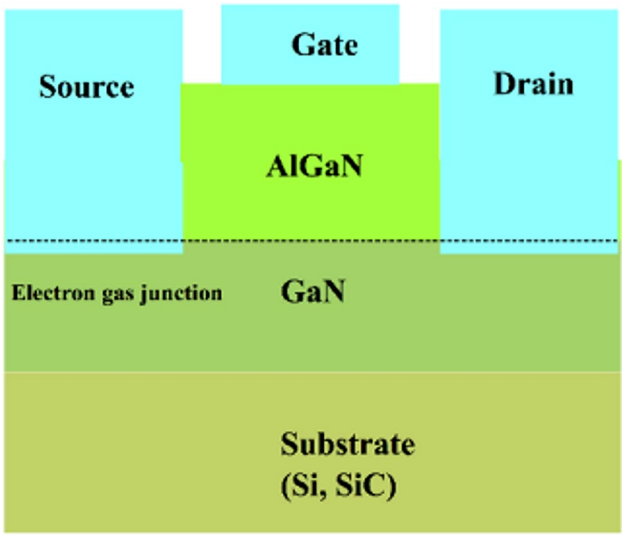


Fig. 22 A GaN-based HEMT with SiC substrate [132]

resistance, enabling efficient, high-power operation. Wide bandgap (WBG) technology further enhances their reliability at high frequencies and temperatures [132].

To further reduce leakage currents in SiC MOSFETs, future advancements are likely to focus on enhancing gate oxide reliability and interface quality. Research into alternative gate dielectrics, such as high-k materials or novel passivation techniques, could lead to significant reductions in gate leakage (I_{GSS}) while improving overall device stability [133]. In addition, the exploration of advanced annealing processes and post-deposition treatments is expected to minimize oxide defects and improve the SiC/SiO2 interface quality, which is critical for reducing leakage currents.

Another promising area for future advancement is the optimization of device design at the nanoscale. The use of nano-structuring techniques, such as the incorporation of quantum well structures or the engineering of nanoscale heterojunctions, could enable better control over leakage mechanisms [134]. Such approaches might lead to a new generation of SiC MOSFETs with dramatically reduced off-state leakage (I_{DSS}) and enhanced on-state performance.

The field of SiC MOSFET research has seen a remarkable surge in recent years, with numerous studies contributing to our understanding of the behavior of these devices and applications. To highlight these significant contributions, summarizes key research studies from the past 4–5 years.

While notable progress has been made, several areas still require further investigation and development to fully unlock the potential of SiC MOSFET technology. A deeper understanding of leakage current mechanisms, particularly at a fundamental level, remains crucial. This includes examining the impact of defects, impurities, and surface states on leakage behavior and enhancing the accuracy of predictive models. Additionally, there is a pressing need for more reliable and standardized testing methods for assessing leakage currents in SiC MOSFETs, especially under extreme operating conditions. Such methods would allow for consistent benchmarking and comparison across different device designs and manufacturers.

Finally, further research should focus on integrating SiC MOSFETs into advanced power electronics systems, such as those used in electric vehicles (EVs), renewable energy systems, and industrial automation. Understanding how these devices perform in real-world applications and under varying environmental conditions will be essential to optimizing their design and ensuring long-term reliability.

8 Conclusion

This review provides an in-depth analysis of leakage current mechanisms in MOSFETs, with a primary emphasis on SiC devices, which are increasingly being adopted in power electronics due to their superior thermal and electrical properties. A central finding is the significant role of gate oxide degradation in driving gate-to-source leakage currents, a phenomenon particularly pronounced in SiC MOSFETs

under high electric fields and elevated temperatures. The most prevalent mechanism identified for gate leakage is quantum mechanical tunneling, with Fowler-Nordheim tunneling and trap-assisted tunneling being key contributors to the gate leakage in SiC MOSFETs. Additionally, the impact of packaging materials, device architecture, and intrinsic defects further aggravates gate leakage, particularly in harsh operating conditions. The study also explores drain-to-source leakage current, revealing that reverse-bias junction leakage plays a substantial role in this type of leakage in SiC MOSFETs. Factors including Gate-Induced Drain Leakage (GIDL) and Drain-Induced Barrier Lowering (DIBL) were also found to exacerbate this issue, especially at higher drain voltages.

Mitigating these leakage currents is essential not only for improving device efficiency but also for enhancing the long-term reliability of SiC MOSFETs, particularly in power applications where thermal management and high voltage endurance are critical. While recent advances have addressed many challenges, further research is necessary to develop more robust gate oxides, innovative packaging materials, and refined device structures. Moreover, advanced simulation models and measurement techniques are crucial for accurately predicting and controlling leakage behavior under real-world operating conditions. Addressing these challenges will be pivotal in unlocking the full potential of SiC MOSFETs in next-generation power electronics systems, enabling higher efficiency, reduced thermal load, and improved reliability across a wide range of implementations.

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